Design and Analysis of Half Adder and Full Adder Using GDI Logic

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Abstract

For low power digital circuits like half adders and full adders, we designed and analysed speed, power, and area using GDI gates and basic CMOS.Simulation software tools like Microwind2 and Dsch2 are used to implement the design for both half adder and full adder. In order to compare different logics for power, speed, and area, we have used CMOS and GDI. In comparison to CMOS logic, we have discovered that GDI logic has produced better results for digital circuits.

Index Terms: Logic Gates, CMOS, GDI, Half Adder, Full Adder.

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INTRODUCTION

The Half Adders and the Full Adders are the two main building blocks in any electronic circuit. The use of electronic devices has grown quickly with the improvements in technology today. The interior area or space of electronic components or devices must be optimised if we want to reduce the size of electronic devices. All integrated circuits' primary building blocks are adders (ICs).We can incorporate more electronic components into a single IC, If we minimise the size of the electronic parts. Considering that we are currently using large-scale electronic devices, low power digital circuit design is necessary. We need to build electronic devices that have less delay and perform faster than outdated technology since we know that as circuits get smaller, performance will increase. Therefore, the goal is to build low power digital circuits that are smaller, less expensive, and have shorter processing times than CMOS technology. Determining the lowest power design solutions for GDI (gate diffusion input) that give low area, power, and speed is therefore necessary. By employing this method, it enables the creation of a broad range of complicated logic functions using only two transistors. It is also possible to use fewer layout components if we have a design that takes up less space. The Half Adder and Full Adder will be designed and implemented utilising simulation software using Microwind and Dsch 2, which is used to build Schematic diagrams and Layouts. The DSCH2 tool was used to create the schematic diagram, and it allows for both direct conversion to SPICE code as well as conversion from schematic to verilog. The Schematic Diagram layout was designed using Microwind, and we may also create using the diffusion method, which allows us to compare power. Using 90nm technology, we can adjust the distance between the source and drain for diffusion.

ADDERS

A digital circuit called an adder processes input data through the gates of each computer to add numbers. Every computer have an adder, which will serve important roles. ALU units utilise adders as a fundamental component of all electronic circuits. Adders can be built for a variety of purposes, including the representation of numbers, the conversion of binary to excess-3 codes, and binary code.

HALF ADDER

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table

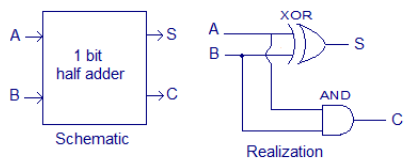

Figure 1: HALF ADDER CIRCUIT

Half adder has 2 inputs (A, B) and 2 outputs (Sum, Carry), respectively. Various types of logic, such as CMOS and GDI logic, are being designed and compared.A and B are the inputs,the outputs however are sum and carry. The output carry is 0 if none of the inputs are 1. The least significant bit of the total is specified by the sum bit. Basic addition can be built with the use of logic gates and a half adder. Let's examine an illustration of the addition of two single bits. Truth table and half-adder circuits are shown in Figure 1.

A 2-bit half adder has the following truth table: Truth Table for Half Adders 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, 1 + 1 =10.There are no other single-bit combinations besides these.The sum, however, needs to be expressed as a two-bit output because 1 + 1 equals 10. The equations are therefore 0 + 0 = 00, 0 + 1 = 01, 1 + 0 = 01, and 1 + 1 = 10.Carry-out is the result of 10. While carry is often the carry-out, sum is frequently the output.

It is now evident that a simple 1-bit adder built by employing an AND Gate for the Carry and a XOR Gate for the output SUM.

The half-adder is highly useful for arithmetically adding binary data with one digit.Making a truth table and reducing it is one method for building adders that can handle two binary digits. The half adder addition action is repeated twice to create a three binary digit adder. When you choose to construct a four-digit adder, the procedure is carried out in a manner similar to that.

With this theory, it became obvious that development takes time, but implementation is straightforward.The exclusive OR function is used in the simplest expression: Logical Diagram: sum = A XOR B, carry = A AND B, The sum and carry's SOP form is as follows: Carry = xy, Sum = xy+xy. Following is the Boolean statement for the half adder circuit: Carry = A AND B (A.B) and Sum = A XOR B. A full adder has two outputs sum, and carry, as well as three inputs A, B, C respectively. Utilizing two half-adders and OR gate, this logic circuit implements a full adder.Usually, a cascade of many adders that add binary values of sizes 8, 16, 32, etc. includes the Full adder.

The circuit produces a two-bit output. The signals Cout and S are frequently used to represent the output carry and sum, with Cout + S serving as the sum.There are numerous ways to implement a full adder, including either by utilising a distinct transistor-level circuit or by utilising different gates.

If the circuit is constructed using straightforward integrated circuit chips with only one type of gate per chip, employing only two types of gates is practical. A and B are connected to the input of a half-adder,utilising Cin as the second half adder's other input and its sum output S as one of its inputs, utilising an OR gate to combine the carry outputs of the two half-adders, and finally connecting Cin to the second half adder's other input, Two half adders can be combined to create a full adder.

The final carry output comes from the OR Gate, and the final sum output (S) of the full adder is the sum-output from the second half adder (Cout). Full adders have a critical path that begins at the sum bits and passes through both XOR gates. The delay caused by a full adder's critical route,assuming that an XOR gate needs to be completed with delays, is equal to A carry's critical path passes through two gates (AND and OR) in a carry block, one xor gate in an adder, and as a result. In the following Figure 2, the truth table and full adder circuit diagram are listed.

FULL ADDER

Figure 2: FULL ADDER CIRCUIT

A circuit known as a full adder has three inputs and two outputs, A, B, C, Sum, and Carry.By taking a carry from the following lower order half adder circuit greatness and sending it to the following higher request extent half adder, two parts can be added to one another. By using cascadeform halfadders, which can generate double numbers in increments of 8, 16, 32, and so on, the n cycle complete adder ought to be feasible. This circuit produces a carry and sum yield that is meaningless, which can be addressed by the signs s and cout. Full Adder is a synonym for the entire thing, and it can be done in many different ways in addition to the logic door.For instance, with specialised transistor level circuits, constructed gates, and unique logic. Sum=A xnor B xnor is one method of full adder execution. In order to address Cin and Convey, use Cout = (an and b) or (cin and (a xnor b)) In this execution, the final OR door prior to the full yield could be replaced by an XOR door without affecting the reasoning that follows. Simple coordinated circuit chips are used to finish the circuit, with the help of which two types of doors can be operated, which contain just one door type for each chip,Using A and B together as the contributions for one half of the adder, its entire yield S as one of the contributions for the second half of the adder, and Cin as its other contribution for the half adder at that point at long last OR entryway yield would convey from the two half-adders taken, it is also possible to build a full viper with the aid of neither entryway. Then, the second half adder's final total yield (S) will be taken, which can then become a full snake. The last convey yield is the yield from the OR entrance (Cout). Given that an XOR door requires one delay to complete, the delay caused by the basic route of a whole snake is similar to the basic route of a bring, which passes through one XOR entryway in a viper and through two doors (in addition) in a convey square. Below Figure [2] displays the truth table and full adder circuit diagram. Based on the inputs listed in the table, it is possible to establish the logical expression of the sum., = A'BCin+A'B'Cin+AB'Cin"+ABCin = Cin(A'B"+AB)+Cin"(AB"+AB") = Cin EX-OR(A EX-OR

B) Based on the inputs shown in the table, it is possible to derive the carry's logical expression (Cout)., = A'BCin +AB"Cin+ABCin'+ABCin = AB+BCin+ACin A half Adder and a full Adder barely differ from one another. Half Adder uses two-bit data sources to produce results,after which the output of the half Adder is used by the full Adder to generate another result.TIn any CPU, the number juggling circuits are built using the Full Adder as the actual square.. It is formed from two Half-Adders.

CMOS Logic

Complementary Metal Oxide Semiconductor is what the word CMOS refers to.This CMOS technology one of the most used in the semiconductor design industry. because it is widely used for a wide range of modern IC applications. Complementary MOS, sometimes known as CMOS, is one of the most well-liked MOSFET technologies currently on the market.

This is the most popular semiconductor technology for ASICs, memory like RAM, ROM, and EEPROM, microprocessors, and microcontroller chips. The substantially lower power dissipation of CMOS technology as compared to NMOS and BIPOLAR technology is its key advantage. Unlike NMOS or BIPOLAR circuits, complementary MOS circuits almost eliminate static power dissipation. Energy is only lost if the circuit really switches.

As a result, more CMOS gates can be integrated into one IC than using NMOS or bipolar technology., improving performance significantly. N-channel MOS and P-channel MOS make up the complementary Metal Oxide Semiconductor transistor (NMOS). NMOS is based on a p-type substrate with diffused n-type sources and drains. Electrons make up the vast bulk of carriers in NMOS.

When a strong voltage is applied to the gate, the NMOS will conduct.Similar to this, when the gate voltage is low, NMOS won't conduct. Since the electrons, which serve as the NMOS's carriers, move twice as quickly as the holes do in PMOS, NMOS is thought to be faster than PMOS.In a P-channel MOSFET, the Source and Drain are diffused on an N-type substrate. Carriers in general are holes.

If a high gate voltage is provided, the PMOS will not conduct. When a low voltage is given to the gate, the PMOS will conduct. Compared to NMOS devices,More noise can be tolerated by PMOS devices.The Basic CMOS Circuit in Fig. 3 was designed to resemble an inverter circuit, and the Basic CMOS Circuit in Fig. 4 was implemented using a digital schematic circuit tool.

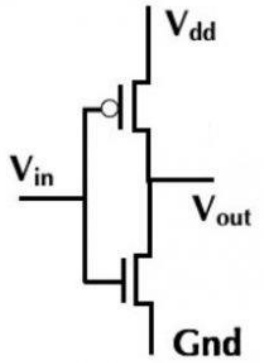

Figure 3: BASIC CMOS

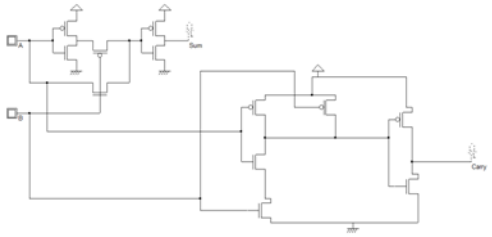

Figure 4: CMOS HALFADDER CIRCUIT

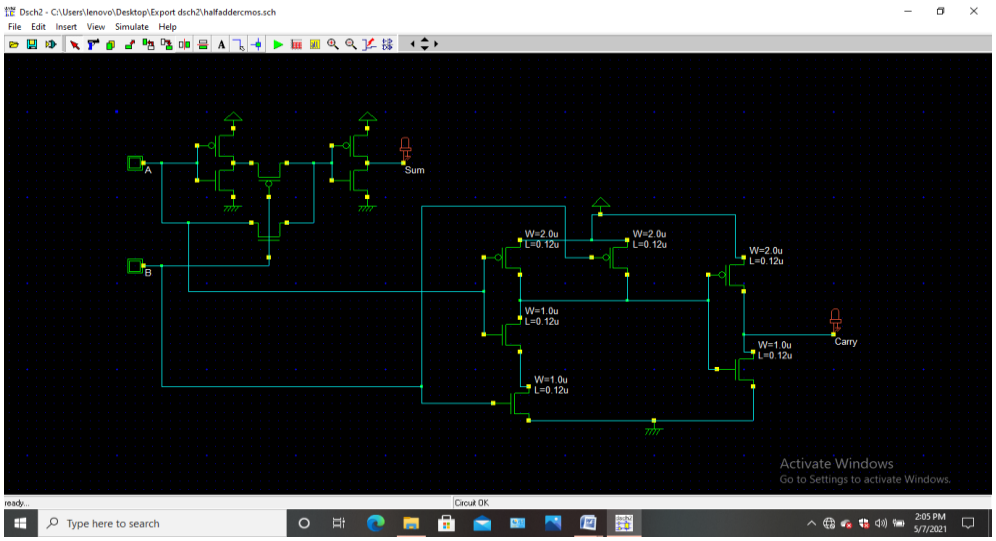

Figure 5: CMOS USING DSCH2

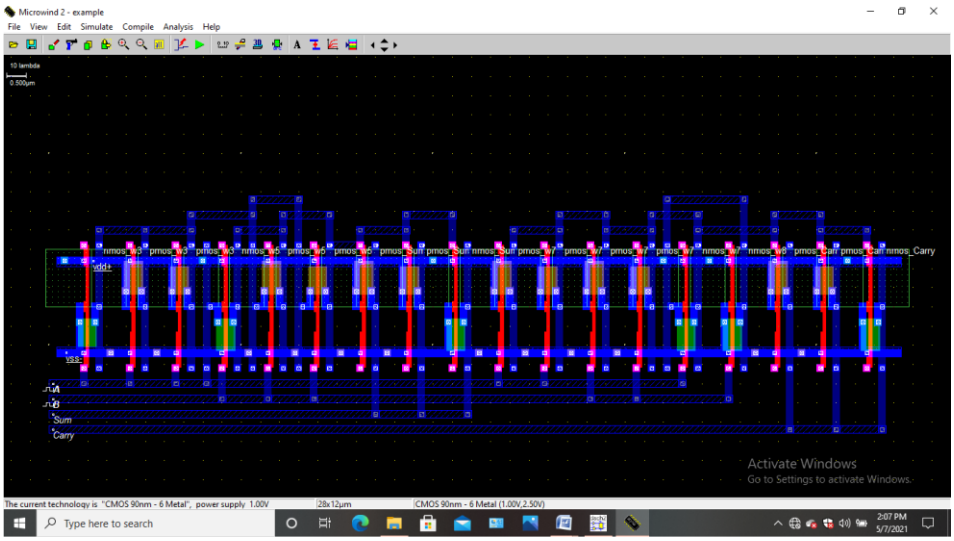

Figure 6: LAYOUT DIGARAM USING MICROWIND

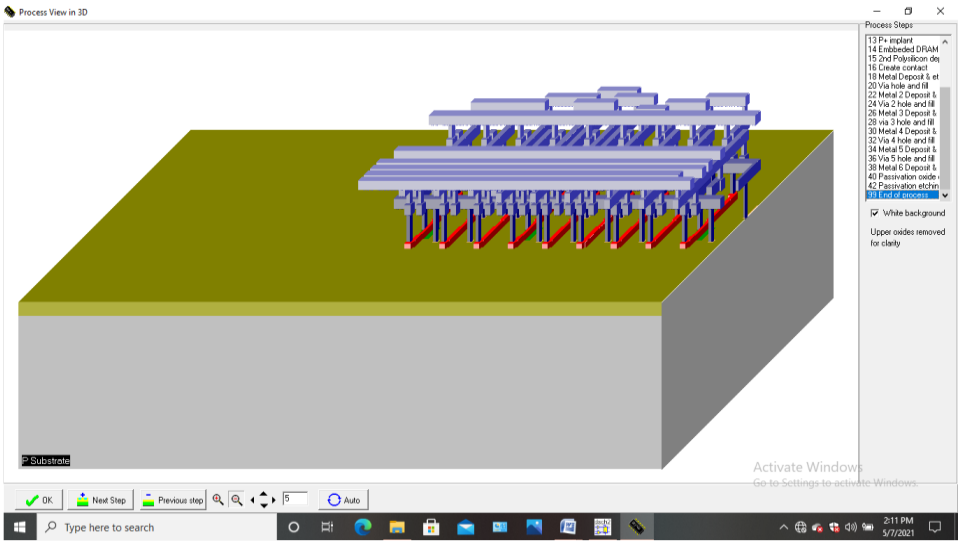

Figure 7: 3D DIGARAM USING MICROWIND

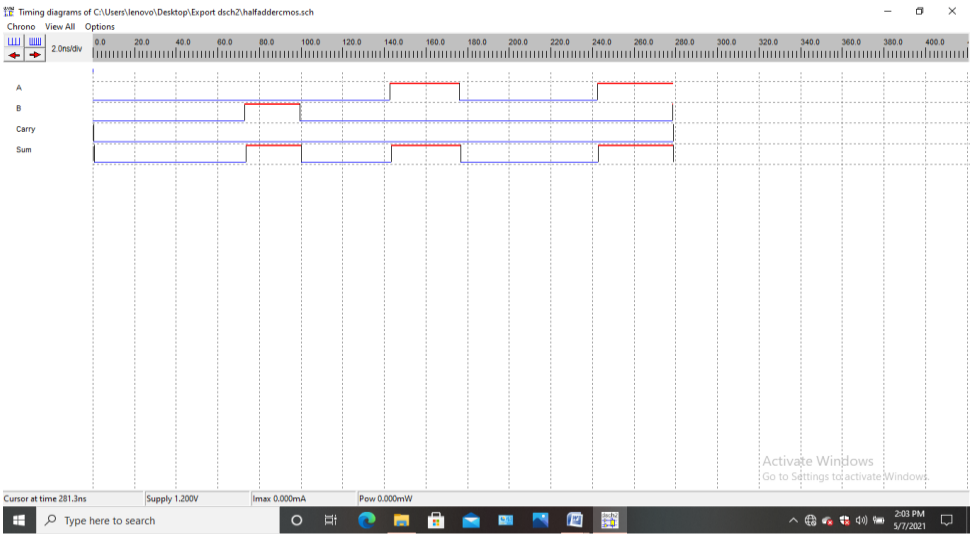

Figure 8: HALFADDER OUTPUT WAVEFORM

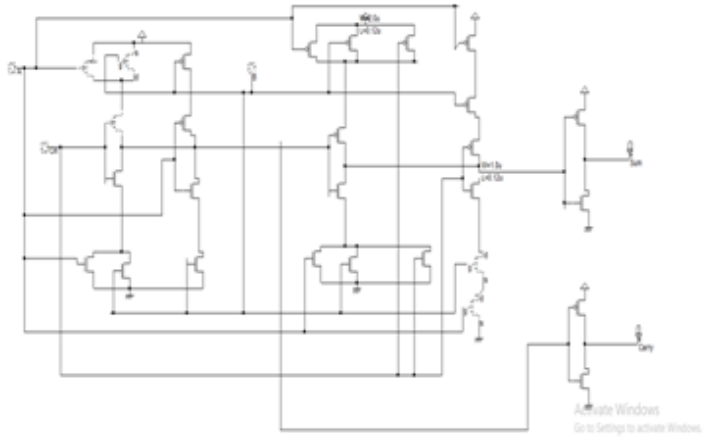

Figure 9: CMOS FULLADDER CIRCUIT

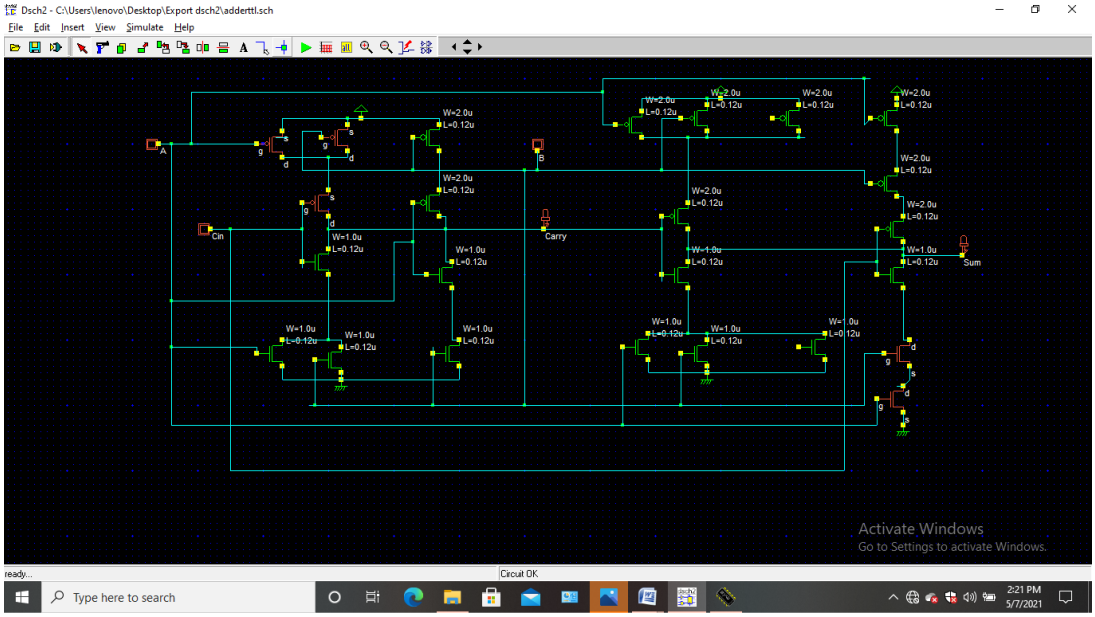

Figure 10: FULLADDER USING DSCH2

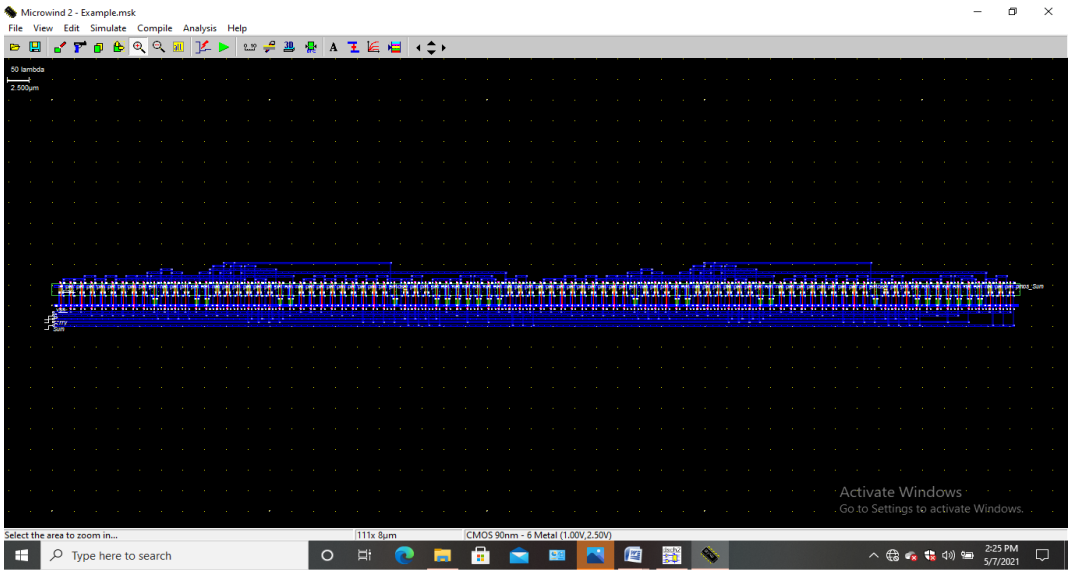

Figure 11: Layout Digaram USING MICROWIND

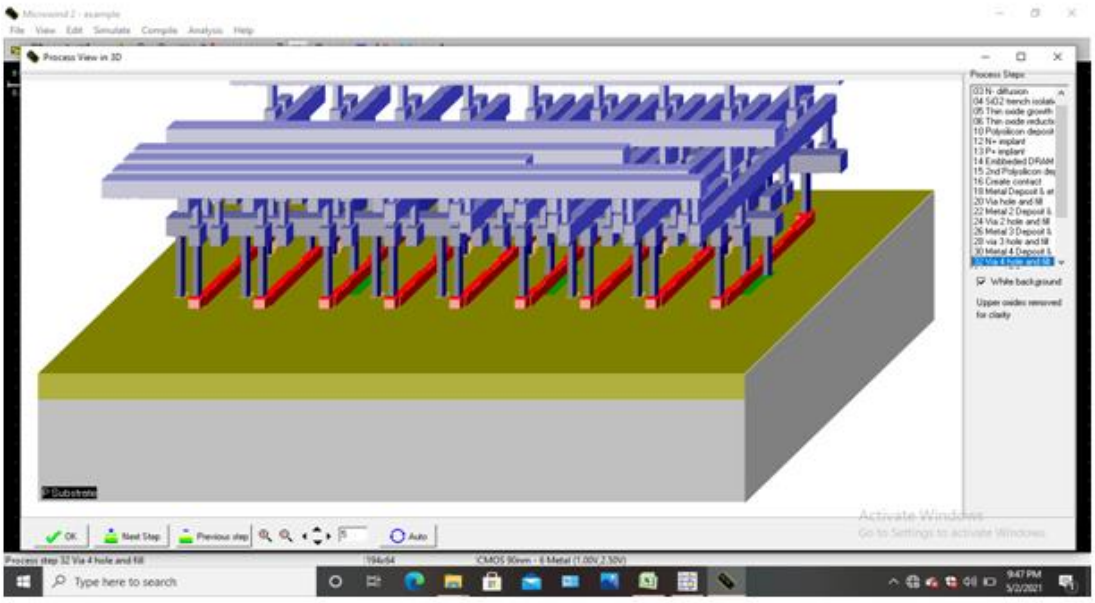

Figure 12: 3D Diagram

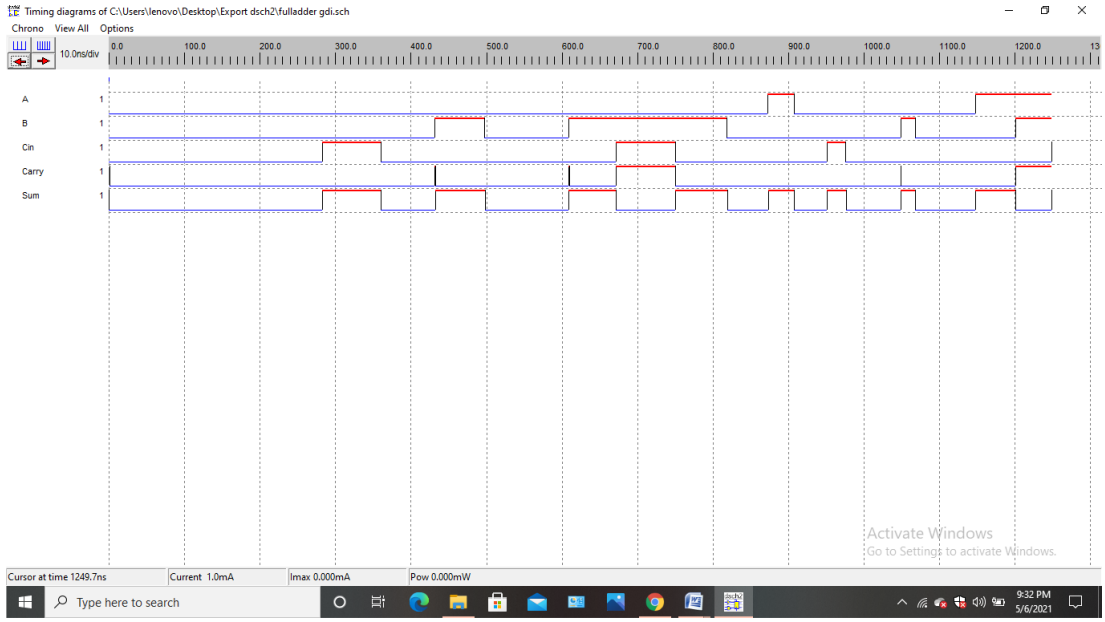

Figure 13: Output waveform

GDI Logic

A further invention that is used for low power plans that require greater force and region is known as GDI, or exchange entrance way dissemination input.For a basic cmos inverter, similar to a GDI, we need three contributions, but, depending on the circuit, a bdd contribution for a p will be connected with either a cmos or a Nmos.As we know that 50% of logic will be used by GDI invertor circuit, where n is also associated with the pmos or nmos depending on the circuit, the majority of capacity should be possible by single semiconductor. A simple CMOS inverter requires three contributions. Over the past 20 years, a number of design methods have been created to enhance the display of logic circuits that rely on CMOS.. In GDI, a triple information technique, P is associated with the source or channel of PMOS in place of Vdd input, and N input is similarly related with the source or channel of NMOS.The majority of PMOS is linked to P information, while the majority of NMOS is linked to N input (see Figure below). CMOS Inverter Using GDI strategy. For a n-input semiconductor the quantity of Inverter CMOS using the GDI approach. The number of contributions in this scenario for a semiconductor with n inputs is n+2.contributions in this instance are n+2. Two

semiconductors are sufficient for the majority of capabilities. The GDI is used as support in 50 out of the situations and is used for logic level reclamation.Improvements have been made in GDI's force scattering, semiconductor tally, and plan complexity. The GDI has a set of drawbacks of its own. Not all functions can be carried out utilising GDI. Even if spilling current is decreasing, there are still GDI cell flaws visible below 90 nm.As autonomous dividers are required between semiconductors, the cell region in GDI is updated. In this study, the GDI cell is introduced, where ground and Vdd are more closely related.As a result of decreasing the gates, latency is addressed in this study.The Basic GDI Half adder circuit is listed in Figure [15] and the Basic GDI Inverter circuit is shown in Figure 14, both of which were created using the Digital Schematic Circuit tool.Figures 16 and 17 above depict, respectively, layout digaram and 3D features.The yield for complete viper circuits is shown in Figure 18. The basic circuit is shown in figure 19. The GDI Full Viper circuit, which was created using the Digital Schematic Circuit tool, is shown in Figure 19.Figures 20 and 21 above depict, respectively, the layout digital and 3D characteristics. The yield for full snake circuits is shown in Figure 22.

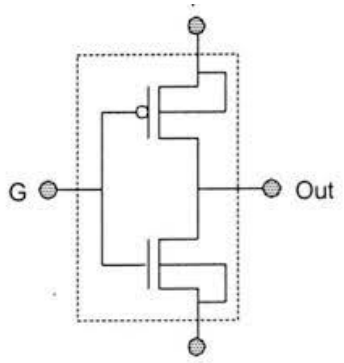

Figure 14: GDI

1. BASIC GDI FUNCTIONS

The GDI Technique Relies on the Use of Simple Cells, as Shown in Fig. 14.From the beginning, the basic GDI cell appears to be a typical CMOS inverter, however there are a few minor differences.

1)The three terminals of the GDI Circuit are G (Normal entry way Contribution of NMOS and PMOS), P (Contribution of NMOS and PMOS), and N. (Contribution to the Source or Channel NMOS). 2) It tends to be self-assertively one-sided at diverging from a CMOS Inverter because the majority of both NMOS and PMOS are related with N or P (separately).Not all of the capabilities can be successfully implemented in a normal P-Well CMOS measurement, but they can be in a twin-well CMOS or Silicon on Cover (SQI) Technology.Simple Chnages of info desgin of the Straightforward GDI Cell relates to Altogether different Boolean Capacities.The majority of these capacities are indicated (6–12 semiconductors) in CMOS, similarly to how regular PTL execution is carried out. However, the GDI PLan Technique is exceptionally straight forward (just two semiconductors are required for each capacity). The majority of these restrictions are complicated (6–12 semiconductors) in CMOS, just like in typical PTL executions, but amazingly simple (just two semiconductors per restriction) in the GDI plan technique. A significant portion of the circuit arrangements in this study relied on the F1 and F2 restrictions. The explanations behind this are provided in the following.

1) F1 and F2 have finished analysing families (licenses affirmation of any possible two-input reasoning work).

2) Due to the persistent and uneven nature of the primary piece in any NMOS, F1 is the only GDI operation that can be recognised in a typical p-well CMOS measurement.

3) The diodes between NMOS and PMOS are driven at high reasoning levels for N and low reasoning levels for P.

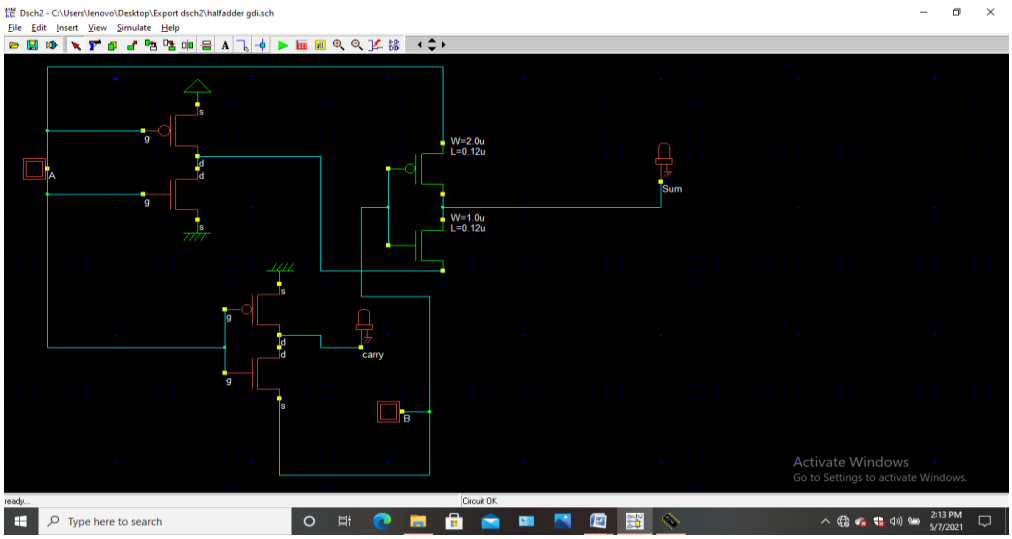

Figure 15: GDI HALFADDER

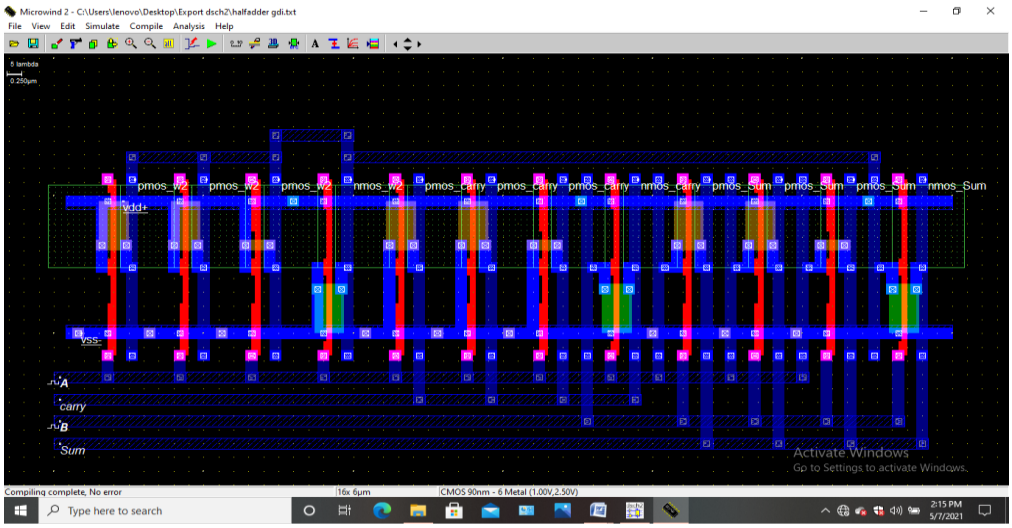

Figure 16: LAYOUT DIGARAM USING DSCH2

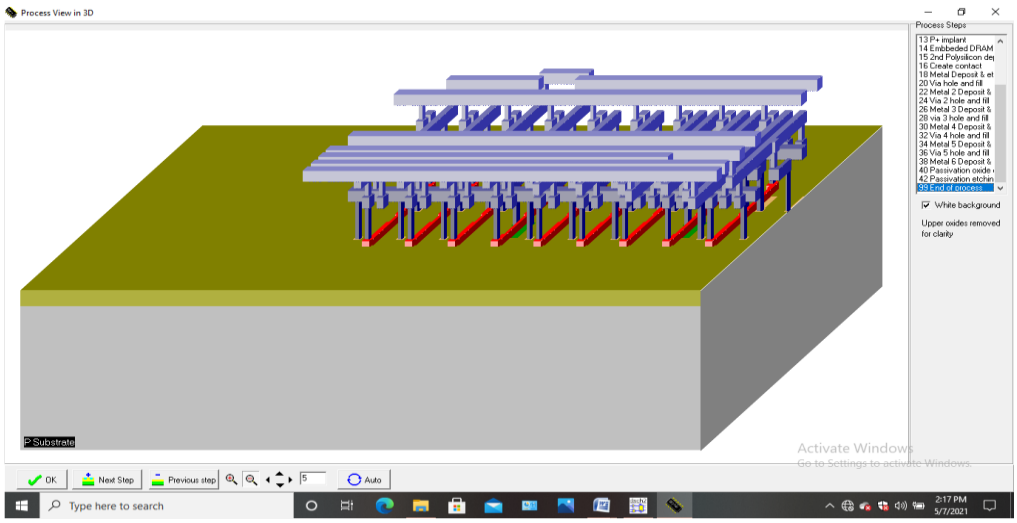

Figure 17: 3D DIGARAM USING MICROWIND

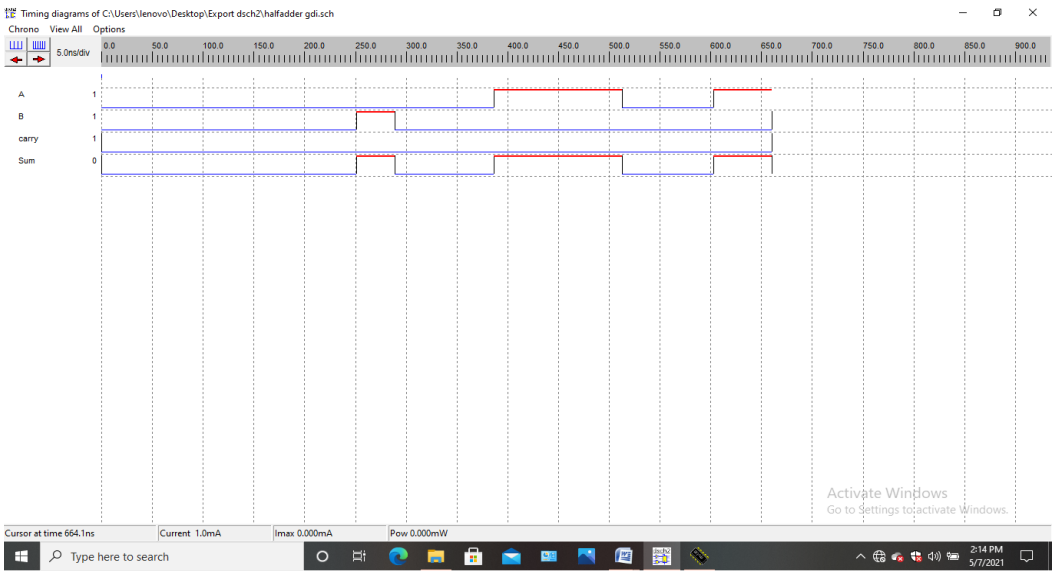

Figure 18: HALF ADDER OUTPUT WAVEFORM

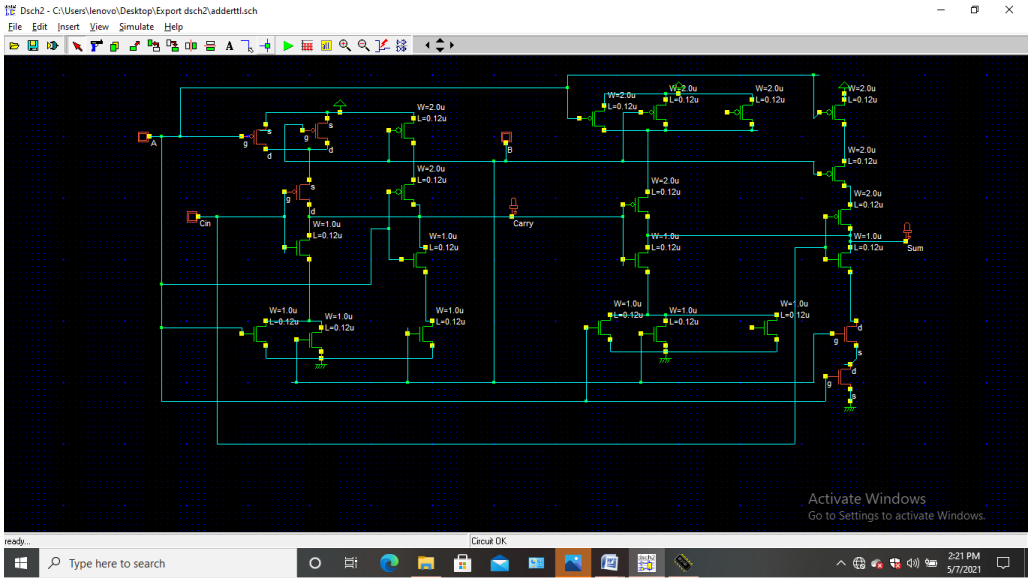

Figure 19: FULLADDER USING DSCH2

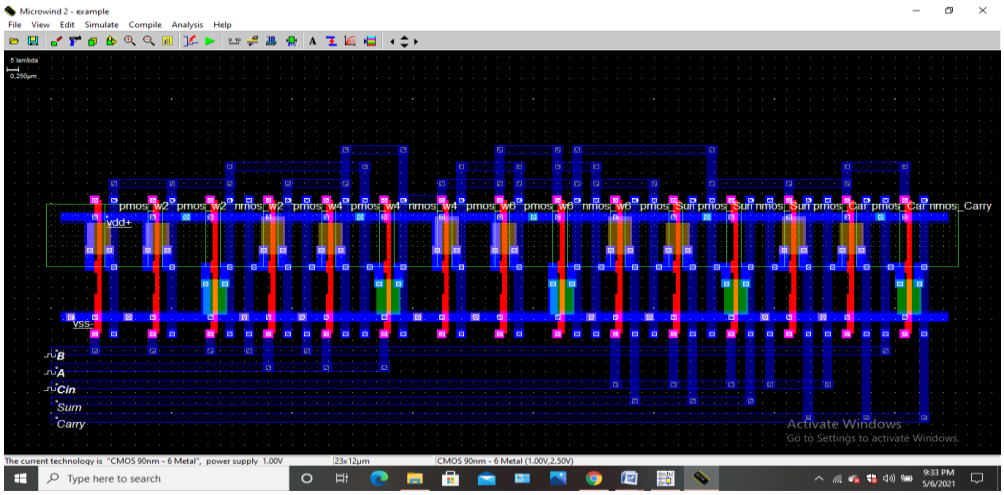

Figure 20: LAYOUT DIGARAM USING MICROWIND

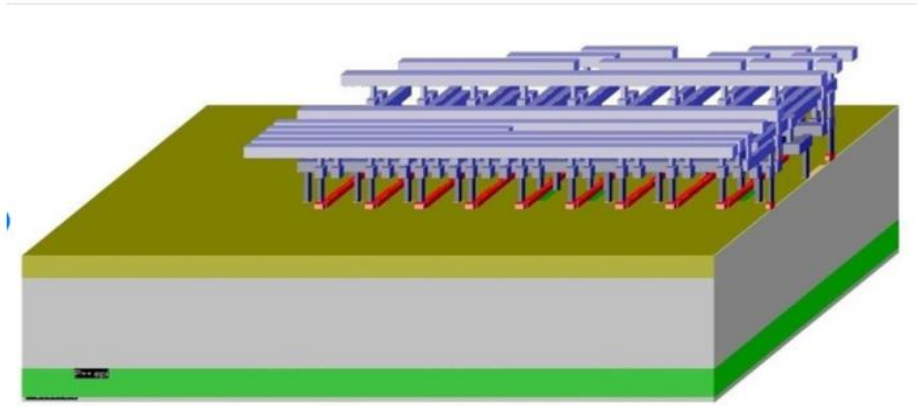

Figure 21: 3D DIGARAM USING MICROWIND

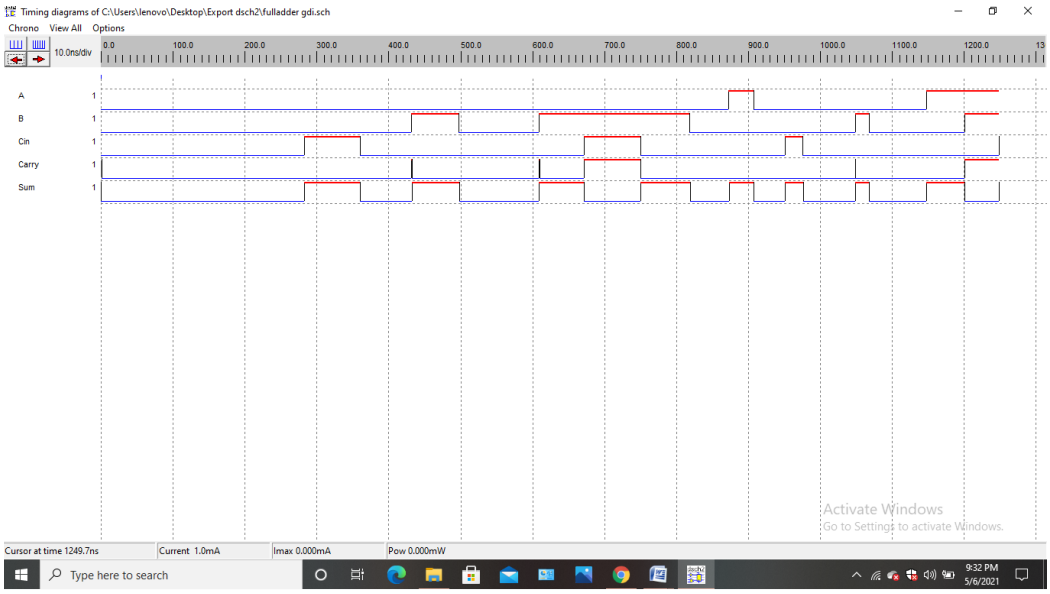

Figure 22: FULLADDER OUTPUT WAVEFORM

METHODOLOGY

Basic logic gates were used in the CMOS-based half-adder and full-adder design and GDI Technology.Half adders and complete adders were created with one Xnor gate and one And gate using these logic gates.Similar to that, CMOS and GDI technology will be used with one Xnor gate, For full adders, there are three AND gates and an OR gate.With the use of software, it is possible to create SPICE and Verilog code as well as schematic diagrams for digital circuits.For your design entity, we are able to calculate area, speed, and power CMOS and GDI are two examples of different logic. So, in order to do this, we need to get Efficient.By applying these fundamental logic gates, we are able to create complex circuits in this product and also investigate a variety of 3D diagrams and features.

SIMULATION RESULTS

The DSCH 2, MICROWIND Tool was used to simulate all of the previously discussed and suggested concepts.There will be designs for both the Half Adder and the Full Adder.using different logic technology, and the outputs were individually tested and verified.shows us the outcomes of digital circuits employing various adders with various input configurations. It also includes a report on the delay, power, and area of half adders and full adders utilising different technologies. Below figures demonstrates the graphical depiction of synthesis reports of delay, power, and area of the Half Adder and Full Adder, which were successfully obtained using prior technology.

RESULTS

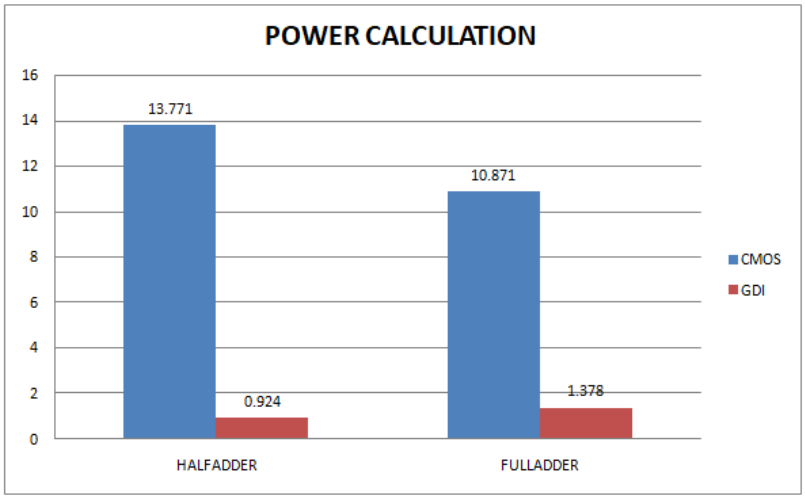

Figure 23: Compared Power For CMOS AND GDI

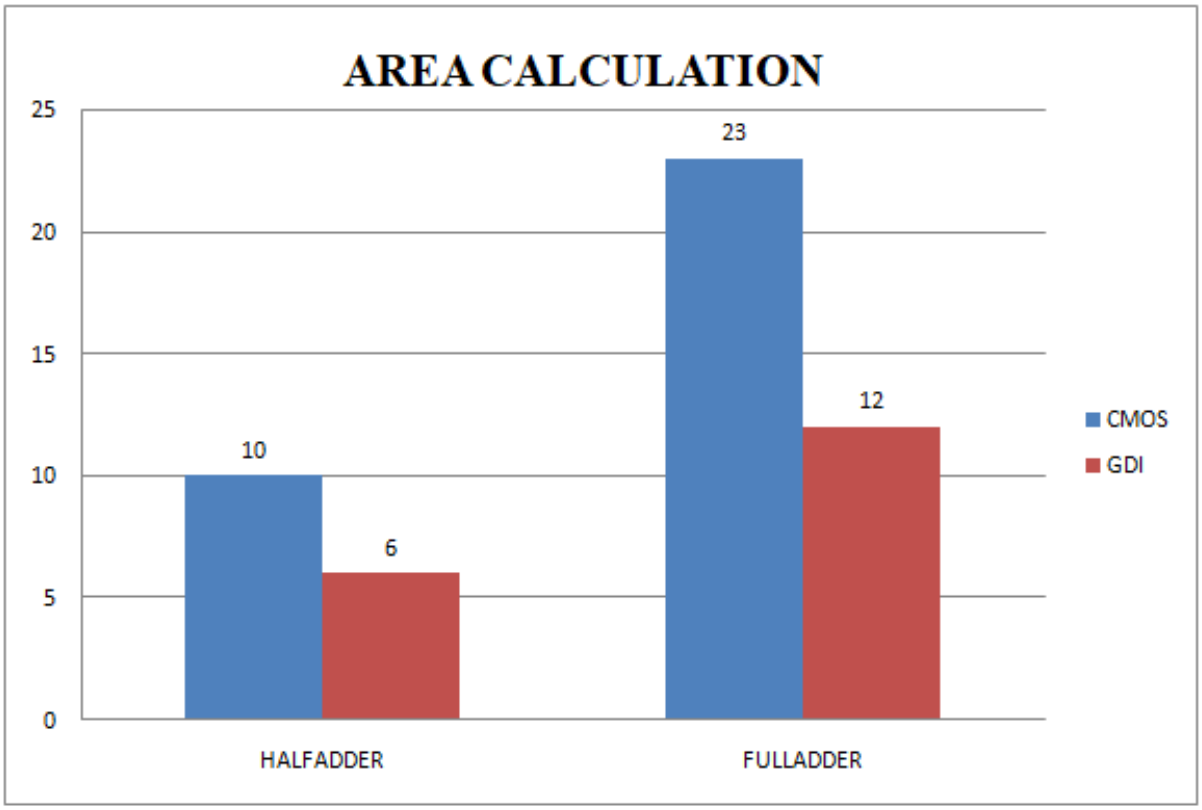

Figure 24: COMPARED AREA for CMOS AND GDI

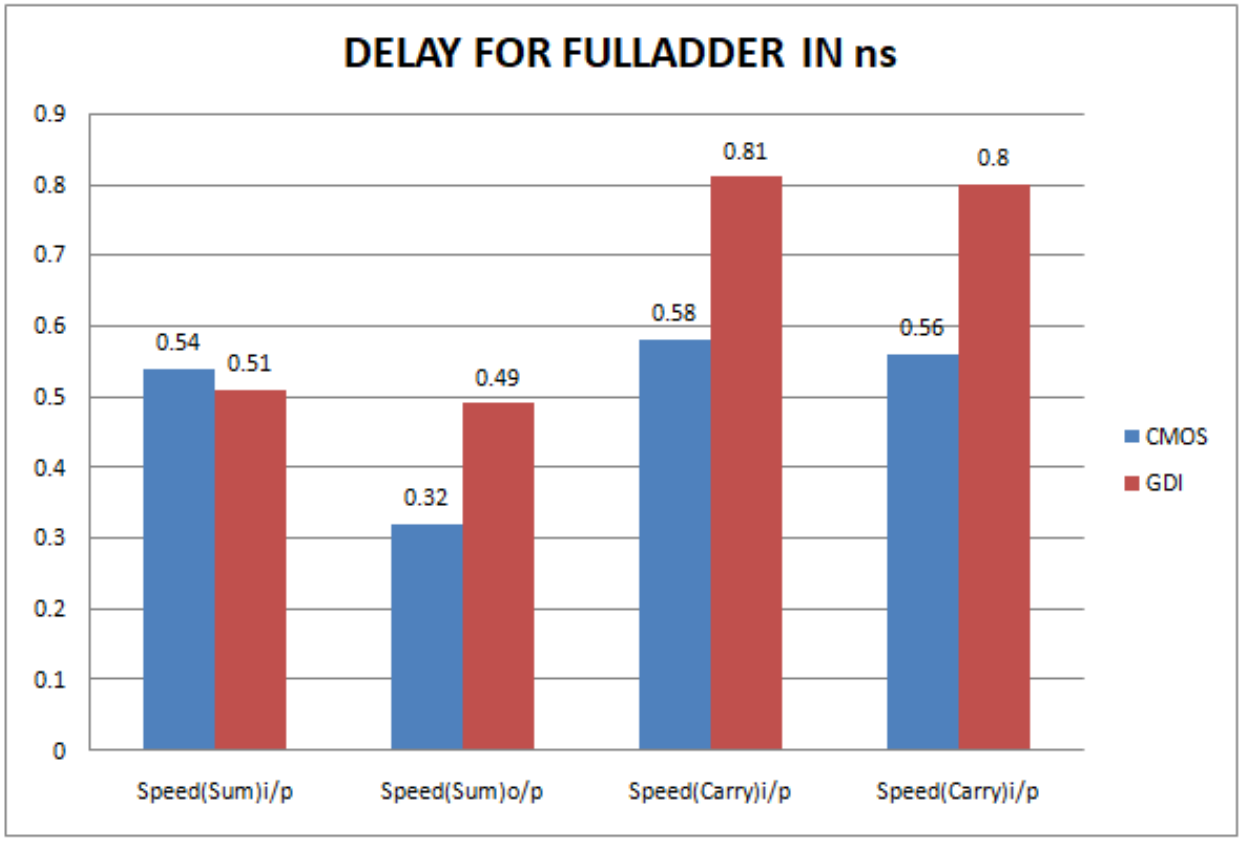

Figure 25: Compared Speed For CMOS AND GDI

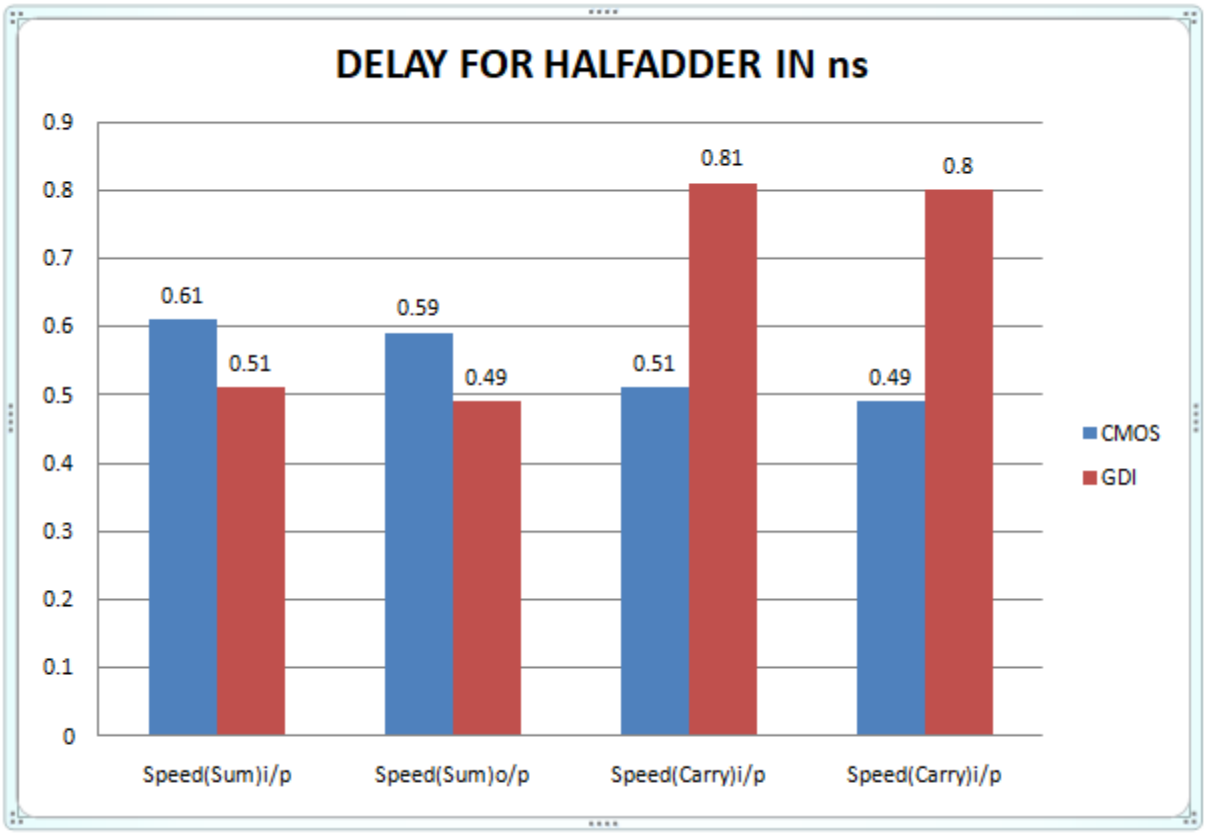

Figure 26: Compared Speed For CMOS AND GDI

Table 1: Comparative Analysis of HALF ADDER IN TERMS OF POWER, DELAY AND AREA

S.NO	LOGIC	DELAY(in nS)	NO OF TRANSISTOR	Power (uW)
1	CMOS	0.20	10	13.771
2	GDI	0.20	6	0.924

Table 2: Comparative Analysis of OF FULL ADDER IN TERMS OF POWER, DELAY AND AREA

S.NO	LOGIC	DELAY(in nS)	NO OF TRANSISTOR	Power (uW)
1	CMOS	0.20	23	10.871
2	GDI	0.02	12	1.378

Conclusion

This Paper proposed and analysed a variety of different technologies, including CMOS and GDI, for power, area, and speed.When compared to CMOS Technology, the Half Adder and Full Adder that are implemented utilising GDI and CMOS logic have proven to be the best in terms of area, power, and delay.GDI logic will faster than CMOS logic And Efficient. The aforementioned adder circuits and vedic multiplier topologies are crucial for designing digital logic. Advanced digital signal processors can be made faster and their ALU size can be optimised by using the Half Adder and Full Adder circuits mentioned above.

References

Low Power Digital Circuits Design Using 120nm Technology, IJSTR Volume 9, Issue 4, APRIL 2020, Nandyal Naveena.

Nagaraj, Analysis of various Adders Using CMOS, CPL, and DPL Logic2017 14th INDICON 438362017 IEEE.

Nagaraj S. 2020 ic-ETITE, 2020, pp. 1–5, "Design and study of high speed and low area vedic multiplier employing carry choose adder."

2020 ICSTCEE, pp. 120–123, Maheshwari, "Fault Tolerant Reversible Full Adder Design Using Gate Diffusion Input," doi: 10.1109/ICSTCEE49637.2020.9276774.

High speed vedic multiplier designs: A review by Yogita Bansal, 2014 RAECS.

Low Power Digital CMOS Design by A.P. Chandrakasan (Kluwer, Norwell, MA, 1995).

2020 ic-ETITE, pp. 1-4, doi: 10.1109/ic-ETITE47903.2020.413, K. Lilly, "Analysis of 32-Bit Multiply and Accumulate unit (MAC) using Vedic Multiplier."

Low power VLSI circuit design methodologies: A literature analysis, S. K. Varadharajan, 2017 ICEDSS, pp. 245-251, doi: 10.1109/ICEDSS.2017.8073688.

Area-Delay Efficient and Low-Power Carry Skip adder for High Performance Computing Systems by Bharat Garg, iSES (Formerly iNiS), 2019, Year: 2019.

NAGANAIK MUDHAVATHU, DR.P.KARPAGAVALLI, "DESIGN OF

HIGH PERFORMANCE ADDER ARCITECTURE USING GDI TECHNIQUE".

Jagruti Makwana, Vishwa Shah and UrvishaFatak, “Design and Performance analysis of 32 Bit VLSIHybrid adder”, 3rd Inte. Confe. Tre. Elec. Info. (ICOEI), IEEE, 2019.

10.1109/ICCMC48092.2020.ICCMC-0004, C. R. Patel, "Vedic Multiplier in 45nm Technology," 2020 Fourth ICCMC, pp. 21–26.

2020 ICESC, p. 929–932, M. B. Murugesh, "Modified High Speed 32-bit Vedic Multiplier Design and Implementation," doi: 10.1109/ICESC48915.2020.9155882.

Somashekhar Malipatil (2017). Review and analysis of Glitch Reduction for Low Power VLSI Circuits IJRASE, ISSN.

Neil H.E.’s book CMOS VLSI Design: A Circuits and Systems Perspective describes how to design digital integrated circuits. all novices.

Basic VLSI Design by Douglas A. Pucknell, Kamran Eshraghian.

User’s Guide for Microwind and DSCH version 3.1, Microwind INSA France, 1997-2007, pp. 97-103, 200.