OriginalArticle

Enhanced Fixed width booth multiplier for improved accuracy

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Abstract

Digital signal processing (Digital signal) applications like the rapid Fourier - transform infrared and discrete transform frequently employ fixed-width multipliers. Fixed-width multipliers in DSP applications truncation the half least a major bits (LSBs) in order to provide an output that is the same widths as the input, which causes an error known as a "truncation error." Here, we propose a multilayered conditional distribution (MLCP) estimator-corrected precision fixed-width Booth multiplier.

Keyword: DSP, MLCP, FWBM

I. INTRODUCTION

Digital signal processors are essential components in a wide range of telecommunication applications for transferring data between devices. FIR filters are used in DSP applications to achieve efficient results, whereas digital multipliers paly major role in DSP processers [1]. Multiplication procedures have the fixed-width feature in many applications involving digital signal processing (DSP) and multimedia. In other words, the bit width of their data inputs and output outcomes match. For instance, only (W-1) least-significant bit are removed to reduce the (2W-1)-bit product of the W-bit multiplexer and W-bit multiplier to W-bits (LSBs). In fixed-width multipliers, the adder cells required for calculation the (W-1) LSBs are frequently removed, and the adder units that are left are given the appropriate biases. Several designs for fixed-width multipliers have been put forth [2]. Discrete impulse response filters and discrete cosine transformation (DCT) are two examples of digital signal processor (DSP) algorithms that frequently include multipliers. The requirement for an easy-to-use yet accurate fixed width multiplying for use in digital image systems has been a topic of discussion for a while [3]. Multipliers are often used in digital image processing (Digital) systems. A lot of space is frequently devoted to multipliers in the construction of a very-large-scale integrating (VLSI) semiconductor.To lower the area cost of integrated circuits, many different techniques use fixed-width multipliers (IC). By reducing the input bits in the multipliers circuit design, the Booth encoder seeks to improve performance. The compensation techniques often use simulated or statistical analysis to determine an adjustable bias from the partial products. Statistical and linear regression-based first order approximation polynomials for the truncation component are offered; nonetheless, significant inaccuracy still exists.. By using additional data from the Booth encoder, some are able to decrease the truncation error; nevertheless, the sophisticated correction results in a significant area penalty. A binary cutoff and extra information from unfinished products are sometimes used to increase cost while lowering truncation error.To cut down on established time and increase accuracy, the probability adjusted bias was introduced. By utilising a conditional probability, the author increases accuracy even further. Finding a high precision compensated approach in corrected multiplier design is therefore crucial [4].

The carry inputs of a reserve adder cells are added with an estimated compensation value via a number of post - failure methods, which have been developed to successfully decrease the truncation error. Either the constant system or the adaptive strategy can yield the value for error compensation. In order to conduct multiplication operations independent of the impact of the present input data value, the consistent scheme pre-computes the estimated regression compensation significance and then feed them to the carrying inputs of the maintained adder cells. Although the constant technique has the benefit of being simpler, the truncation error is rather substantial.The adaptive scheme, on the other hand, was created to increase accuracy over the constant scheme while slightly increasing hardware complexity by adaptively modifying the compensation value in accordance with the input data. To effectively minimize the insertion loss of fixed-width altered Booth multipliers directly, however, most adaptive error compensation algorithms were established primarily for fixed-width element multiplier [5].

A direct-truncated multiplier, one of several fixed-width multipliers, ignores the half of such partial products array that includes the less important bits. It significantly shrinks the region while producing a huge truncation mistake. Contrarily, post truncated multipliers round off the product after fully accumulating all partial product bits, giving them the highest

accuracy at the price of the most expensive hardware. Numerous gaffe circuits have been developed to reduce the truncation errors in order to obtain a balanced system between precision and hardware costs [6]. Here, we provide a fixed-width Booth multiplier with accuracy adjustments that tried to correct the random errors using an MLCP estimate.

II. LITERATURE SURVEY

In addition to Yuan-Ho Chen, [7] this summary offers a near MLCP equation with column data that may be utilised to adjust accuracy in response to system requirements.By using this method, long Booth multipliers may be performed with excellent accuracy without the need for lengthy and laborious simulations. A versatile, affordable, high-accuracy fixed-width Booth multiplication might be created using the suggested MLCP compensating circuit.

Wen-Quan He et al. [8] propose a simulation- and probability-based fixed-width Booth multiplication.The probability approach is used to produce a number of pre-design solutions utilising anticipated and conditional expected values. Then, based on SNR simulation, the which was before solution with the best accuracy is chosen. The suggested PACS includes an error compensation method as opposed to systems that rely just on simulation. Regarding accuracy or circuit performance, the PACS Booth multiplier beats virtually all of the previously mentioned alternatives. The PACS is also more adaptable and reliable in terms of accuracy.

An adaptive conditional-probability estimator (ACPE) in corrected Booth multipliers is suggested by Yuan-Ho Chen et al. in their paper from page 8 [9]. Without using heuristics, the ACPE is developed from conditional-probability concept, which may be simply used to long Booth multipliers to get improved precision. In order to adapt the accuracy in light of system requirements, ACPE additionally induces the column information w. PSNR and area cost performance for the 2-D Discrete cosine implementation with ACPE Booth multipliers show great results. The proposed ACPE thus offers a variable and very accurate compensating circuit applied to a fixed-width Booth multiplier.

The reduction of truncation error that affects fixed length Booth multiplier designs was suggested by DHIVYAR.et al. [10]. Fixed width booths multiplier with multi-level conditioned probability value corrects the Stop mistake. To estimate the truncation error and attain higher accuracy levels, the suggested multilevel conditional probability employs only non-zero code.The proposal also includes a straightforward, compact multilevel conditional probability adjusted circuit. The suggested multilayer conditional booth multipliers must operate with minimal cost and good accuracy. They used the MLCP approach with 1.8V of power compensation to quickly and accurately estimate the Stop error. Therefore, a fixed width Booth multiplication with high precision, cheap cost, and flexibility may be created using an MLCP circuit.

A fixed-width Booth multiplier design is presented by MeshramP. S. et al. [11] based on the anticipated and conditional probability. Using the compensation circuit's architecture as a starting point, we created a helpful method to determine the compensation value. Thus, the suggested circuitry may be quickly developed without the requirement for expensive simulations, even for 64-bit or 32-bit applications. In the suggested method, XOR gates are used to generate the compensation value straight from the input series.The most significant benefit of the suggested strategy is that the solution helps in reducing this idea's effect on overhead delay and high speed. Actually, compared to the MLCP approach, the suggested PACS produces the best circuit performance. The suggested method's excellent accuracy and efficiency is yet another significant benefit.

Dr. Durga Prasad According to et al. [12], mistakes play a significant role in many digital applications, including FFT, convolution, and other ones. Since truncation mistakes and absolute errors are the most common when computing partial products, it is crucial to minimize these errors. This project's main motivation is to reduce absolute mistake, therefore when we consider a 5-2 expander with CSA, we observe that multiplication takes less time and produces less absolute error. In an effort to observe several aspects, we are completing this task.

Wen-Quan He et al. [13] proposed a particular fixed-width Booth multiplier based on the probabilistic analysis of the input series. We initially created an appropriate mechanism for calculating the compensation value before developing the compensation circuit. The recommended circuit's design is so straightforward and doesn't require in-depth simulations, including those for 64-bit or 32-bit applications.The suggested approach directly generates the compensation value from the input series using XOR gates, in contrast to earlier devices.The main benefit of the suggested technique is its fast speed, which lessens the impact of delay overhead. Except for the D-T technique, the suggested CPIS actually provides the best circuit performance. Another significant benefit is that, with the exception of the D-T approach, the suggested method obtains highly accurate and the best accuracy-efficiency. In conclusion, this is a unique and excellent design.

Summary:

- Aside from the D-T approach, certain methods attain high precision and the maximum accuracy-efficiency.
- DSP applications, particularly those that need a high level of precision, can benefit from the usage of DST.
- The SPEB Booth multiplication is advised for use in highly accurate small area VLSI designs.

III. PROPOSED METHOD

Here, using a multilayered conditional probability (MLCP) estimator, we suggest a fixed-width Booth multiplier that is accuracy-adjusted to take into account truncation error. The MLCP method creates a closed - form solution with various bit width L and column information w, enabling quick setup of the compensating circuit and modification of accuracy by changing w.The proposed MLCP delivers estimates by using all nonzero coding, which exhibits high amounts of inter correlation, in contrast to the conditional technique for ACPE, which employs one nonzero coding to calculate truncation errors.

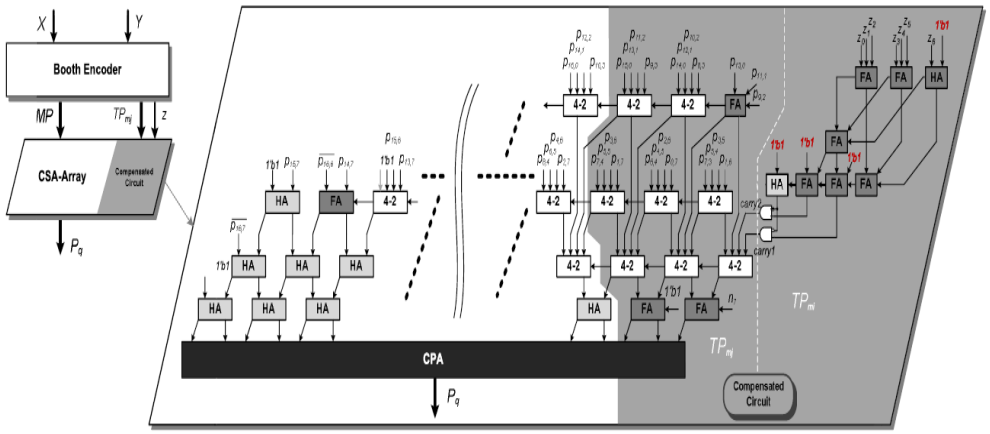


Figure 1 demonstrates the design of the potential MLCP Booth multiplier [11].

i)MLCP ESTIMATOR

In order to easily locate the compensated circuit and adjust the accuracy, the MLCP technique generates a constraint with various bit width L and information columns w. The accuracy of the MLCP approach is better than that of an adapted conditional probability estimator.Even while the adaptive conditional estimator is more efficient, the MLCP technique is more complicated to estimate the truncate error [10].

The quantum products Pq for a multiplier with fixed width may be written as follows:

$$P \approx Pq = MP + TP = MP + \sigma \cdot 2L \text{ (1)}$$

where MP is the primary component of the multiplier, which computes outcomes using real partial products; Fixed width multiplication will be used to truncate the truncation component (Fig. 1, dark region), and stands for the corrected biased of the MLCP estimate, which is made up of TPmj and TPmi portions by conducting the rounding operation. Round ()

$$\sigma = Round\ (TPmj + TPmi) \text{ (2)}$$

The suggested MLCP approach may be used to estimate the minors term TPmi while the main term TPmj gives accurate information. Thus, by calculating TPmi and deriving TPmj, the compensating bias may be added.

ii) A MODIFIED BOOTH MULTIPLIER WITH A FIXED-WIDTH

Here, we'll suggest a fixed-width Booth multiplier with accuracy adjustment that corrects the insertion loss using a multilayer conditioned probability (MLCP) estimator.

It is common practise to use modified Booth encoding to minimize the amount of incomplete products [9]. In two's complement form, a 2L-bit product P may be written as follows:

$$X = -x_{L-1}.2^{L-1} + \sum_{i=0}^{L-2} xi.2^i \text{ (3)}$$

$$Y = -y_{L-1}.2^{L-1} + \sum_{i=0}^{L-2} yi.2^i \text{ (4)}$$

$$P = X * Y \text{ (5)}$$

As shown in Table I, the Booth encoder may transfer three concatenated inputs—y2i+1, y2i, and y2i-1—into yi. Whether or if yi equals zero determines the value of the nonnegative codenzi, a 1-bit digit.In the partial product array created by Booth encoding, if L is an even integer, there are Q=L/2 rows. As an example, the associated partial products for the 8*8 Booth multiplier are shown.

Table1. DIFFERENT BOOT ENCODER

y2i+1	y2i	y2i-1	yi	nzi
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	2	1
1	0	0	-2	1
1	0	1	-1	1
1	1	0	-1	1
1	1	1	0	0

$$P = MP + TP. \text{ (6)}$$

The greatest precision rounding process is used to provide the 8-bit Methods of detecting termed as post truncated (P-T) to the output P. However, VLSI design uses the most circuit area since it calculates all partial products. The direct truncate (D-T) strategy reduces the TP to reduce area cost; nevertheless, a considerable truncation error is produced since the sub - bands from the TP to MP are ignored.Numerous academics have presented a variety of error compensating bias strategies to address truncation error [4].

The quantized products Pq can roughly be derived from (7) to obtain the compensated function:

$$P \approx Pq = MP + \sigma \times 2W \text{ (7)}$$

Where the adjusted biases from the TP to the MP is shown by the symbol.

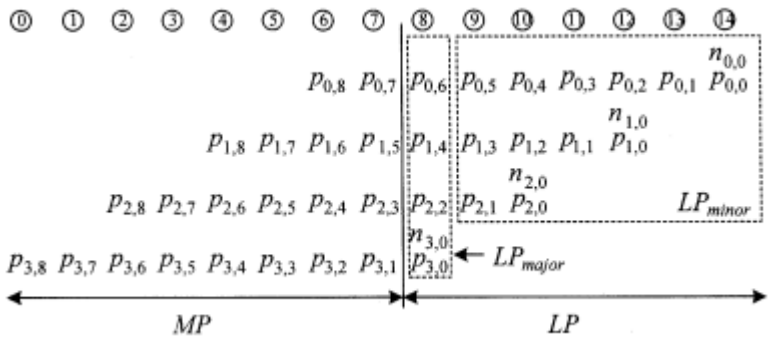


Figure 2 illustrates the MP and LP for an improved Booth multiplier with W = 8.

Figure 2 demonstrates that LPmajor, which has the biggest value in the LP portion, has a dominant influence on the carrying signals produced from the LP component. Furthermore, the outputs of the Booth encoder directly affect the resulting partial products [2]. In this section, an error compensation strategy is suggested based on these observations.

$$S_{LP} = S\_LP_{major} + S\_LP_{minor} \quad (8)$$

Following is a definition of the suggested error compensating bias.

$$\sigma_{prop} = C_E\,[S\_LP_{major} + C_A[S\_LP_{minor}]] \text{ (9)}$$

Where CA[t] denotes the somewhat approximate carrying value for t and CE[t] denotes the precise carrying value of t. The estimated carry value from LPminor to LPmajoris computed in (9), as shown by the notation CA [S -LPminor].

ii) Performance Comparisons

The correctness and circuit efficiency of corrected Booth multipliers are covered in this subsection. To help with comparisons of the accuracy of low-error Booth multipliers, Tables VI–VIII include the average absolute error, maximum available error, and SNR. The terms the and are defined as follows:

$$|\varepsilon| = E[|FP - FPa|]/2L \text{ (10)}$$

$$\varepsilon max = \max\{|FP - FPa|\} \text{ (11)}$$

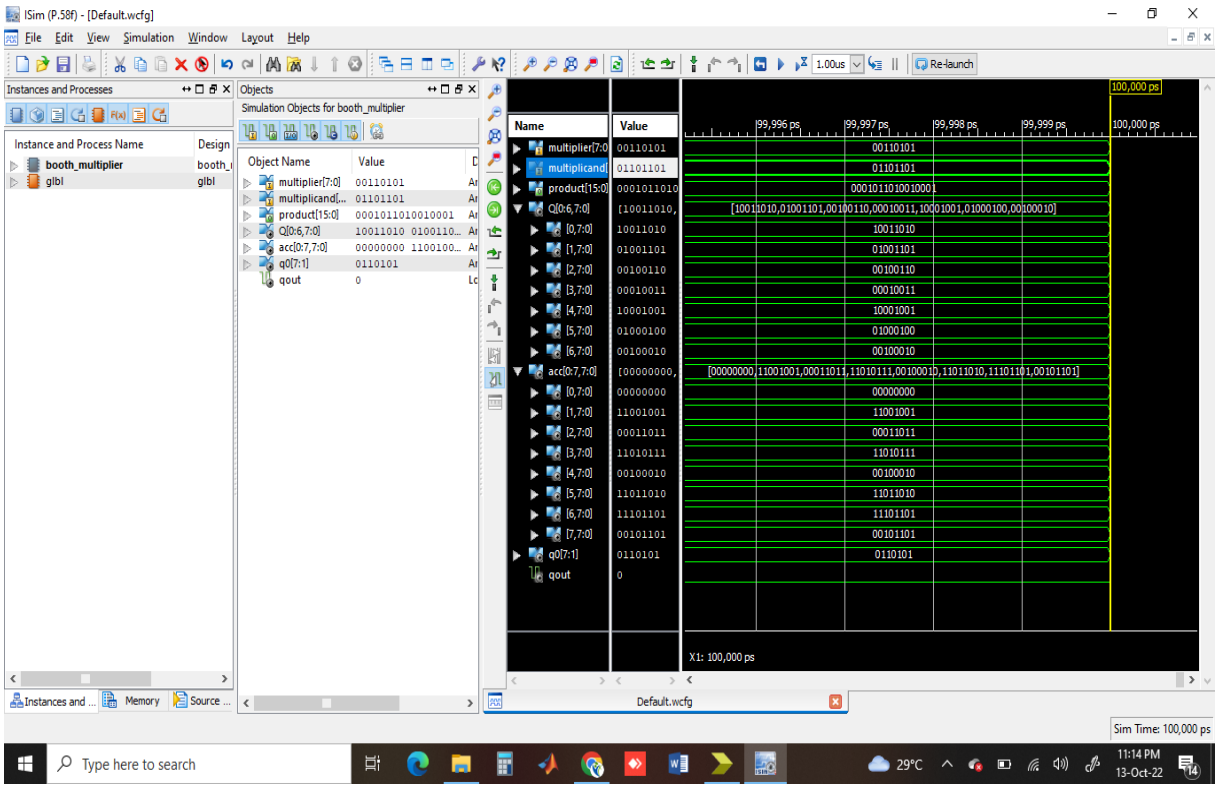


Figure3. Simulation result of proposed multiplier

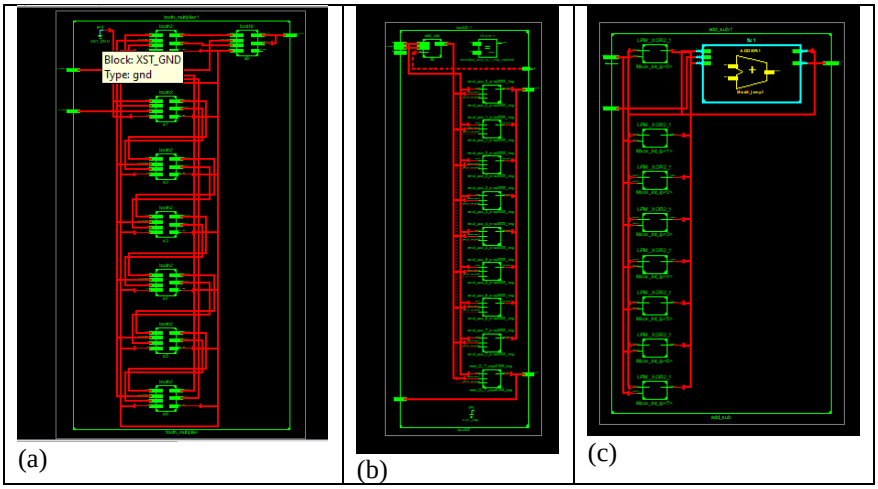


Figure4. RTL schematic of proposed method (a) Proposed Booth Multiplier, (b) booth sub module and (c) adder/subtractor module

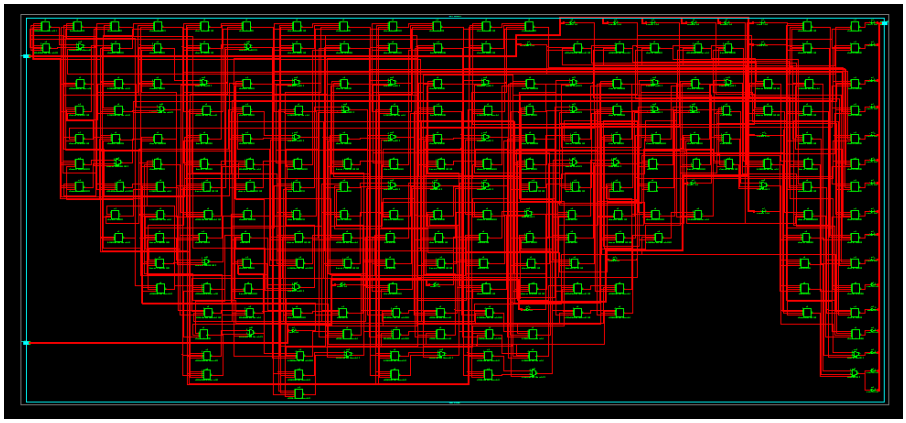


Figure5. Technology schematic of proposed model

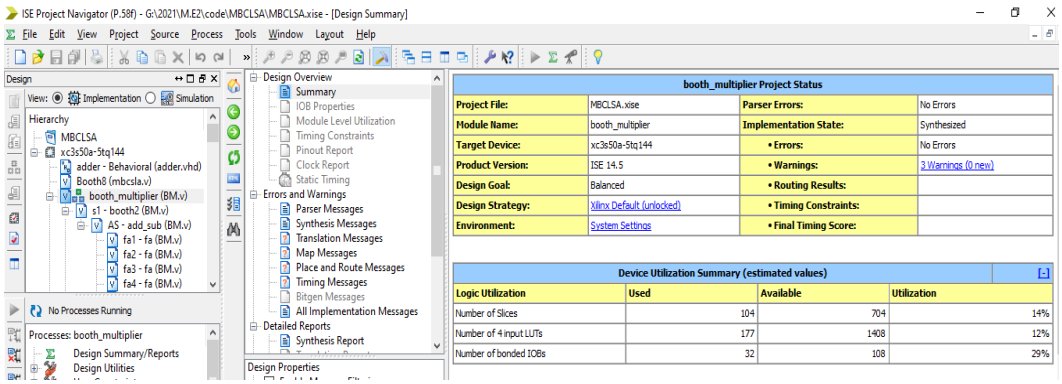
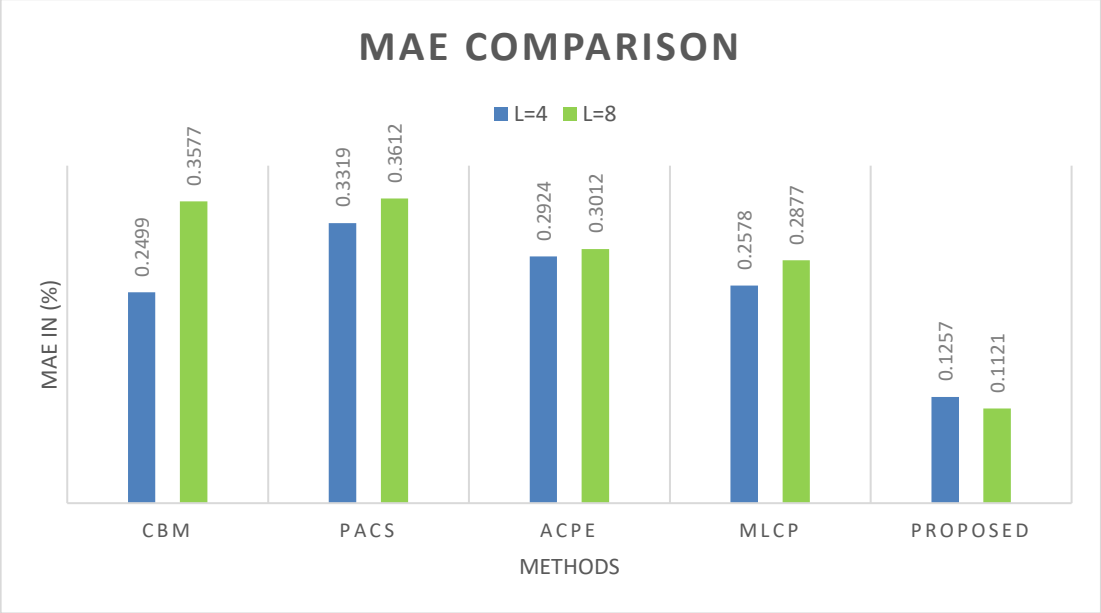


Figure6. Design summary of proposed model worked on Spartan 3AN with XC3s50A

Table2 compares the values of the mean absolute errors for several approaches.

Method	L=4	L=8
CBM	0.2499	0.3577
PACS	0.3319	0.3612
ACPE	0.2924	0.3012
MLCP	0.2578	0.2877
PROPOSED	0.1257	0.1121



Here, we'll suggest a fixed-width Booth multiplier with accuracy adjustment that corrects the insertion loss using a multilayer conditioned probability (MLCP) estimator.

IV. CONCLUSION

Errors play a significant part in many digital applications, including DSP and other applications. Since truncation mistakes and absolute errors are the most common when computing partial products, it is crucial to minimize these errors. Here, we propose a multilayer conditional distribution (MLCP) estimator-based corrected Booth multiplier with accurate modification that corrects the power losses. Using a multilayered conditional distribution (MLCP) estimator, we developed a fixed-width Booths multiplier in this work that takes truncation error into account.And the results show how well our dependable fixed-width Booth multiplier performs. Future lossy applications can employ the recommended multipliers to reduce systems size and power use while maintaining output quality.

Future scope : The above proposed methodology can be adopted to PSO optimization base image processing methods which may present a better system[14].

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