Original Article

Design And Implementation Of Bcd Encoder Based Reversible Priority Encoder Using Toffoli Gate

Bindu Batta[1]*, S. Rambabu[2], Dr. Y. Mallikarjuna Rao[3], M. Mahesh Kumar[4], N. Sreenivas Rao[5]

[1]* M.Tech (VLSI), Santhiram Engineering college, Nandyal, E-mail:- bindumadhuri610@gmail.com
[2] Assistant Professor, Santhiram Engineering college, Nandyal, E-mail:- Rambabu.ece@srecnandyal.edu.in
[3] Associate professor, Santhiram Engineering college, Nandyal, E-mail:- hod.ece@srecnandyal.edu.in
[4] Assistant professor, Santhiram Engineering college, Nandyal, E-mail:- maheshkumar.ece@srecnandyal.edu.in
[5] Assistant professor, Santhiram Engineering college, Nandyal, E-mail:- sreenu.ece@srecnandyal.edu.in

***Corresponding Author**: - Bindu Batta

*M.Tech (VLSI), Santhiram Engineering college, Nandyal, E-mail:- bindumadhuri610@gmail.com
Doi: 10.47750/Pnr.2022.13.S05.314

Abstract

An essential component for encoding and decoding numbers is a reversible priority encoder, which is designed in this study. Binary-coded decimal (BCD), a promising nanotechnology, may provide a framework for reversible circuit implementation. This work proposes a simple BCD platform-based bidirectional 4 to 2 prioritized decoder design. The low-cost Toffoli gate design is suggested for use in reversible encoder circuit implementation. The suggested designs are assessed structurally using the BCD Designer simulation.

Keyword: binary-coded decimal (BCD), Toffoli gate, reversible logic.

I. INTRODUCTION

Modern ICs are enormously complicated due to decrease in device size and increase in chip density involving several millions of transistors per chip. The rules for what can and cannot be manufactured leads to a tremendous increase in complexity due to the amount of power dissipation is increased [1].Priority encoders and comparators are fundamental and significant computational units in digital systems. A priority encoder produces just one output that is "1," with the other outputs all being "0"; this output represents the highest priority. The amplitude of two input values may be determined using a comparator. Additionally, a priority encoder may be incorporated into the construction of a comparison and is the primary element that affects performance [2].

In addition to other uses, priority encoders are employed in a variety of computer systems. It must be decided whether to permit a single request to access such a resource when many processes, modules, or units make use of the same hardware (or software) resource. The resource is made available to the request with the primary concern thanks to the priority encoder's implementation of a fixed selection function. Buses, fixed and float point unit, I-O, data converters, and successfully met router are a few examples of subsystems that utilize encoder functions. These subsystems can have between 16 and 64 inputs [3].

It has been suggested that a number of hierarchical designs be used to handle larger PEs with sizes up to a few thousand bits. Examples include a method that uses a collection of one-hot encoders or a collection of certain comparator and sort circuits. However, their architectures need a lot of resources to keep a good running frequency (FREQ). To build a scalable, high-performance PE, we thus present a set of concepts in this work that extends our prior 1D to 2D transformational leadership is based PE [4].The high - risk and low encoders are regarded as a significant subclass of encoder technologies that have lately received a lot of attention in the literature. As a result, the staircase array structure of the priority encoder is based on a dynamic pre-charge/pre-discharge technique. With the inclusion of the necessary balanced price standards circuitry, this dynamic method is seen as an extra overhead logic and the delay for big size encoders is not much reduced [5]. Applications for reversible logic can be found in quantum computing, nanotechnology, and the best possible information processing [6].

Very humongous integration (VLSI) is in great demand at the design levels of architectural, circuit, and processing technology. By using the right logic while implementing combinational circuits, power consumption may be decreased. The cause is because these logic designs have a significant impact on power consumption, changeover rate, switch capacitance, and short-channel effects. Thz operational frequency can be attained if the device functions with electrons, and VLSI-based device production continues to decrease the sizes smaller to atomic scale. However, a trade-off between the featured size and the increasing demands of performance limits must be made [7].

II. RELATED WORKS

The 4-to-2 Priority Encoder's Clifford+T-based implementation was demonstrated by Laxmidhar Biswal et al. in [9]. In the design phase, we turned them into fault resilient architectures by utilising the functional strength of the Clifford+T library. We have also employed low T — intensity templates to keep the runtime below the convergence of extremely fragile quantum states, which further increases the efficiency of these circuits. The fault-tolerant design is a crucial part of the quantum computer, not to mention the other components.

The 4-bit reversible comparator is a low power, high performance device that was first presented by AbikayalK. et al. This 4-bit changeable comparator is built using priority encoding in reversible logic gates. Feyaman, Toffili, and BJN gates make up the reversible comparator's suggested design. The suggested reversible comparator design was compared to earlier designs that were optimised for the quantity of constant inputs, quantity of garbage outputs, quantity of quantum cost, quantity of power reduction, and quantity of delay. These circuits were validated using xilinx ISE program after being developed in verilog. This may be utilised in a number of low power applications.

A reversible quant 2n-to-n BCD prioritised encoder circuit was presented by NusratJahan Lisa et al. [10], where n is the quantity of output bits. The 2n-to-n BCD prioritized encoder circuit's suggested architecture demonstrates that it is made up of quantum NOT gates and OR quantum circuits. We outline an approach for creating a minimal atomic 2n-to-n BCD priority decoder circuit. The research also suggests a method to determine how complicated quantum circuits' quantum gates are. In terms of qubits, delays, garbage output data, constant inputs, complexity of the quantum gate calculation, area, and power, our circuit outperforms the existing ones. For instance, the suggested quantum 8-to-3 BCD prioritised codec circuit has 41.25% fewer quantum gates, 46.05% fewer delays, 48% fewer garbage outputs, 60% fewer constant inputs, and 41.25% fewer area and power requirements than the existing circuit. Additionally, we simulate the suggested quantum Binary prioritized encoder circuit using Finite element analysis DSCH 2.7, demonstrating the circuit's functionality.

WANG, Jun-Chao, et al. The BCD encoder is one of the basic and widely-discussed components of digital circuit design. In this study, we offer a novel reversible BCD prioritized encoder architecture with a quantum cost of 80 that comprises of 5 CNOT & 15 TOFFOLL gates. The selectivity and low power consumption of this Binary encoder created using reversible logic make them clear benefits for wireless sensors.

VandanShukla and others [11] One method to lessen the heating issues brought on by the increased component density on a single chip area is to develop reversible logic circuits. This encourages scientists to create reversible computers for conditions with preferably no power loss. We have suggested a concept for a decimals to BCD encoder employing a BJN reversing gates gate for additional component minimization.Keyboard encoders frequently employ the arithmetic to Binary encoder circuit. This encoder circuit, which makes use of reversible logic gates, may be used to investigate the creation of further reduced power lost devices.

Among others, Sheba Diamond Thabah [12] A D2BE receives a lot of attention for optimization because of how widely used it is in digital circuit designs. When compared to utilising the standard basic logic gates, the circuit uses less power thanks to the reversible logic architecture. In this article, we suggested two methods for creating a D2BE with reversible gates. In term of GC, GO, and QC, the solutions are more effective than the current designs mentioned in this study. When compared to previous procedures, the GO has already been decreased by 72% and 53%, respectively. The primary factor for minimising power and heat is lost in a circuit is lowering GO. So, a low power system may make advantage of our D2BE architecture.

With the use of quantum physics, KaustavGhosh et al. [13] suggested ideas based on the idea of ternary reversible logic. In terms of energy dissipation and speed, the binary reversible circuit outperforms the digital one. The fundamental ternary gates are employed in this study to construct the adder/subtractor, encoder, and priority encoder circuits while accounting for quantum characteristics such quantum cost. Future research can employ the proposed circuits to create sophisticated computing units.

Summary:

- It is possible to create sophisticated computing units using some circuits
- It is possible to use the D2BE design for low power applications.

III. PROPOSED METHOD

i) Toffoli gate

Toffoli gates are only a (3, 3) bi-directional gate, as seen in figure 3 below from source [11]. This gate has a quantum cost of 5.

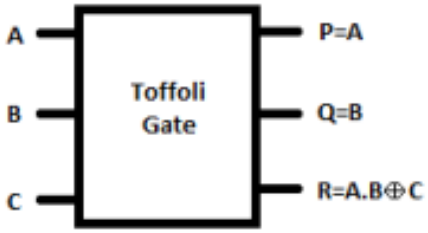

Figure 1 shows a block diagram and the Toffoli gate's output equations.

Controlled Swapping NOT (CSWNOT) gate is another name for the Toffoli gate.

Three inputs and three outputs make up the 33 reversible Toffoli gates (TG) [34]. The TG diagram may be seen in Fig. 6a, where the inputs are A, B, and C and the outputs are P, Q, and R. The outputs are denoted by the symbols "" and "" which stand for binary AND and binary XOR transactions, respectively. They are P = A, Q = B, and R = A B C.TG has a quantum cost of 5 [7].

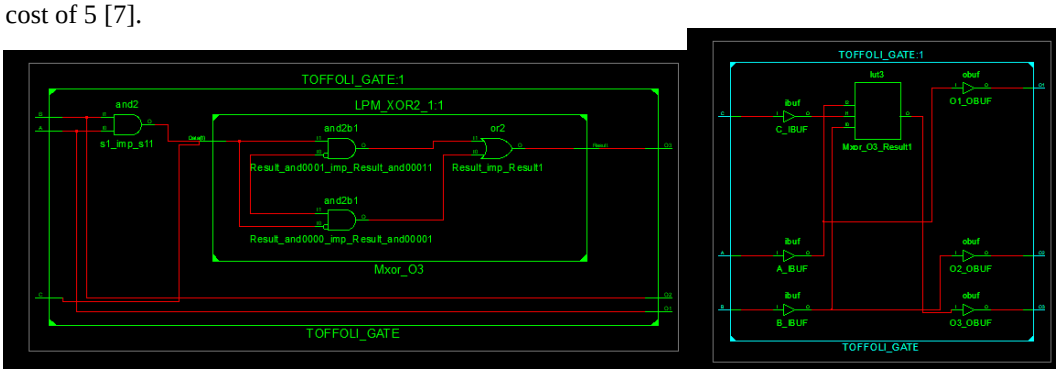

Figure 2. RTL and Technology Schematic of Toffoli Gate

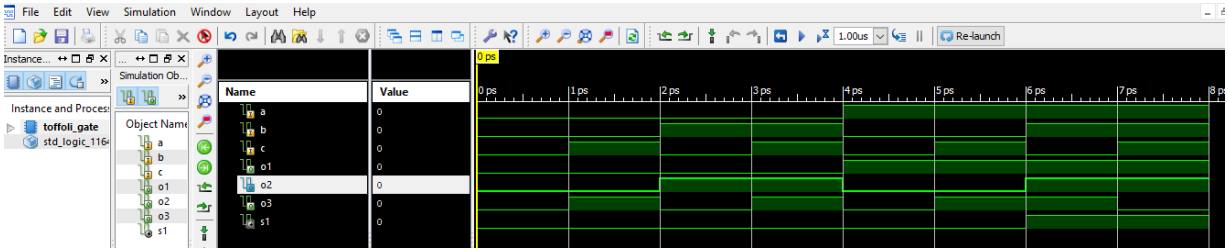

Figure3. Simulation results of Toffoli gate

ii) PRIORITY ENCODER (PE)

A circuit or method known as a priority encoder condenses several binary inputs into fewer outputs. The binary number of the original integer, beginning from 0 of the most important contributing bit, is the result of a priority encoder. By responding on the encoder with the greatest priority, they are frequently employed to manage interruption requests. The input with the top priority will be used if two or even more entries are provided simultaneously. A single-bit 4 to 2 encoder example, where the highest-priority inputs are to the left and "x" denotes an irrelevant value, meaning that any input value there will result in the same result since it will be overridden by higher-priority input. Whether the input is legitimate is shown by the output V [9].

Consider the previous example, where (M, N) comprises numbers like (2, 32), (32, 2), (8, 8), (4, 16), and (16, 4). Therefore, choosing the best pair of (M, N) is crucial for building high-performance PEs.

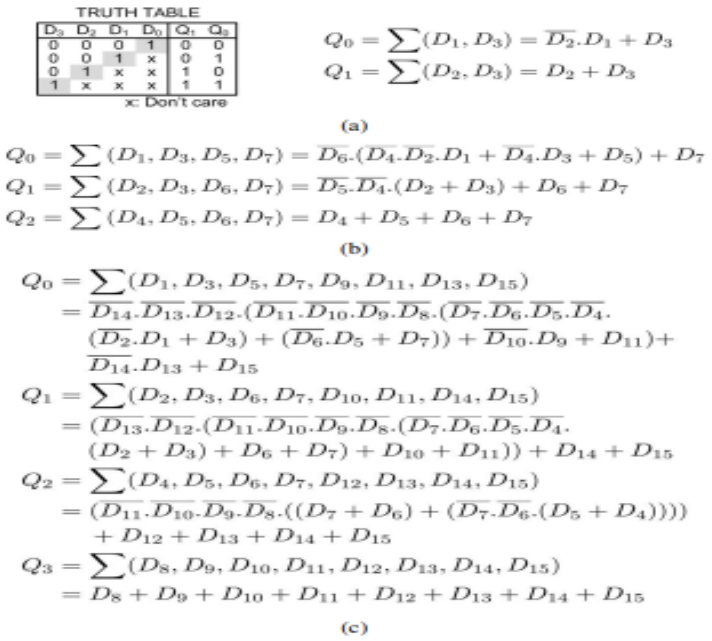

Figure 5 demonstrates the table and the logical statement for PE4 (a), PE8 (b), and PE16 (c).

Fig. 4(a) shows a PE4's truth table with Boolean expression. Similar to this, Figures 2(b) and Figure 2 displays the formulae for such an 8-bit PE and then a 16-bit PE, separately (c). We can see that when PE size ranges between 4-bit to 16-bit, expression complexity skyrockets, making a 32-bit PE solution potentially impractical. As a result, PE4, PE8, & PE16 are again utilised for creating large-sized PEs. Specifically, we evaluate (M, N) at L of 64-bit and (8, 8), (4, 16), and (16, 4).

iii) Decimal to BCD encoder

In essence, there are 10 numbers in a decimal system (0 to 9). A D2BE, which has 10 two inputs and four output lines, can represent these integers (0 to 9) in BCD format. D0 through D9 are used to represent the input lines, whereas A through D are used to represent the output lines. The output equations for a D2BE circuit are as follows:

$$A = D8 + D9. \quad (1)$$

$$B = D4 + D5 + D6 + D7. \quad (2)$$

$$C = D2 + D3 + D6 + D7. \quad (3)$$

$$D = D1 + D3 + D5 + D7 + D9. \quad (4)$$

The traditional gates are used to verify the aforementioned equations. Power loss is an innate characteristic of conventional logic computing. Reversible gates computation can lessen the power loss in the digital circuit's computing as a fix.

iv) Proposed Reversible BCD Priority encoder

In comparison to the traditional 842IBCD encoder, the BCD encoder's function is prioritised, which is a crucial advantage. The significance levels of the remaining inputs decline one at a time, with input 10 having the lowest relevance level and input 17 having the greatest priority level. When T7 is given a greater priority level than T4, for example when in7 and T4 both are "I" while the remaining inputs are all "0," the encoder will disregard T4 and treat the scenario as if only T7 is "I" and all the other input are "0." In Table IT, the BCD encoder's truth table is displayed. A value of "X" indicates uncertain input values.

BCD prioritized encoder truth table, Table 1

INPUT								**OUTPUT**		
I7	I6	I5	I4	I3	I2	I1	I0	C	B	A
1	X	X	X	X	X	X	X	1	1	1
0	1	X	X	X	X	X	X	1	1	0
0	0	1	X	X	X	X	X	1	0	1
0	0	0	1	X	X	X	X	1	0	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	0	0	1	0	0	0

The idea of significant deviation is the initial criterion we adhere to in order to rebuild the BCD precision encoder using reversible logic. 20 more inputs are used, 13 of which are "1"s and the rest are "0s." As a result, only 3 of the determined by a number are genuine, while the remaining outputs are "g" nodes, or nodes containing garbage information. Additionally, the use of irreversible logic gates, such as AND gates and OR gates, is forbidden. For this reason, we transformed the operations of a normal priority BCD encoder into a format that can be quickly translated into a circuit design [14].

The same method was used to complete the redesigning of the reverse BCD input signal, as illustrated in Figure 3, we were able to acquire the reverse circuitry for the operations of B, C, and D rather rapidly.

In their 2012 article, "a BCD Prioritize Encoder Designed by Reversal Logic," Jun Chao Wang, Yu Pang, and Yang Xia described a circuit for encoding a decimal to BCD using reversible logic. This circuit utilised 15 Toffoli gates and 5 CNOT gates for a total quantization cost of 80 [20].Combining several reversible logic gate topologies allowed us to greatly improve the encoder circuit described in section III. We suggested two design alternatives employing just 2X2 or 3X3 circuits since including exponential order reversible logic, such 4X4 or 5X5, will increase the production of trash and hinder the optimization in terms of energy loss. In order to create this circuit, with an overall improvement of 80, we used 5 CNOT gate and 15 TOFOLLl levels, as is evident in the electrical circuits below.

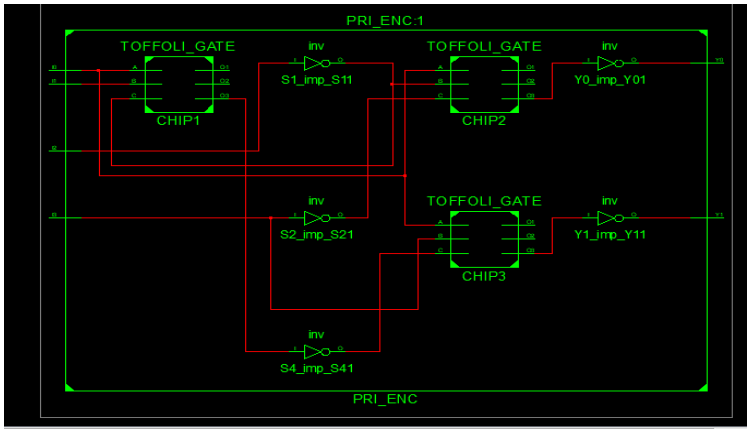

Figure 6. RTL schematic of Proposed 4 bit Reversible Priority encoder with Toffoli gate

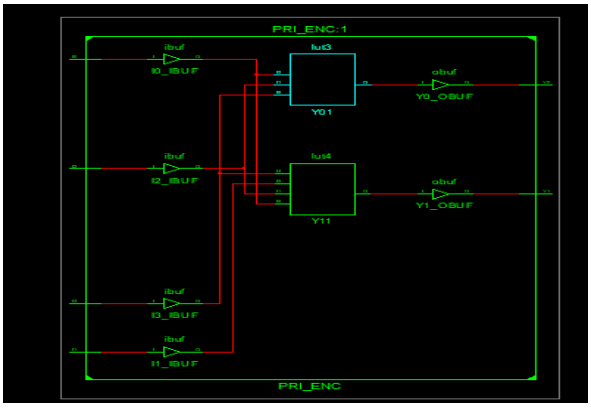

Figure 7. Technology schematic of Proposed 4:2 bit Reversible Priority encoder with Toffoli gate

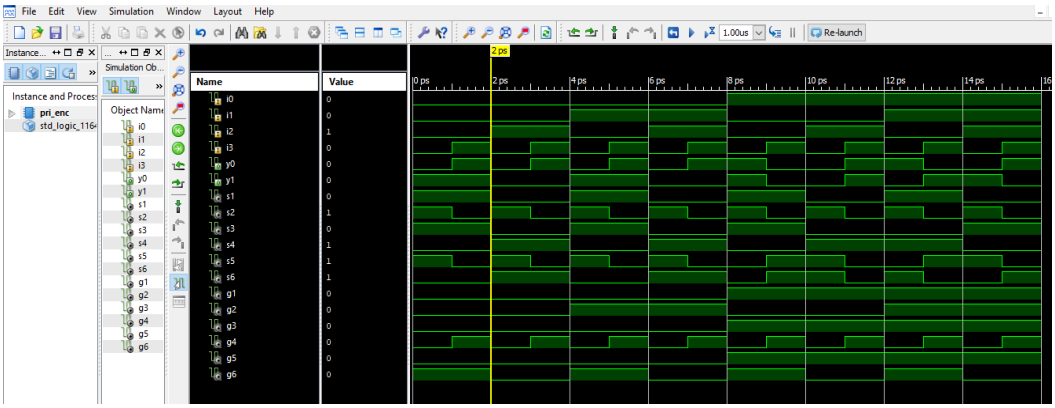

Figure 8. Simulation results of Proposed 4:2 bit Reversible Priority encoder with Toffoli gate

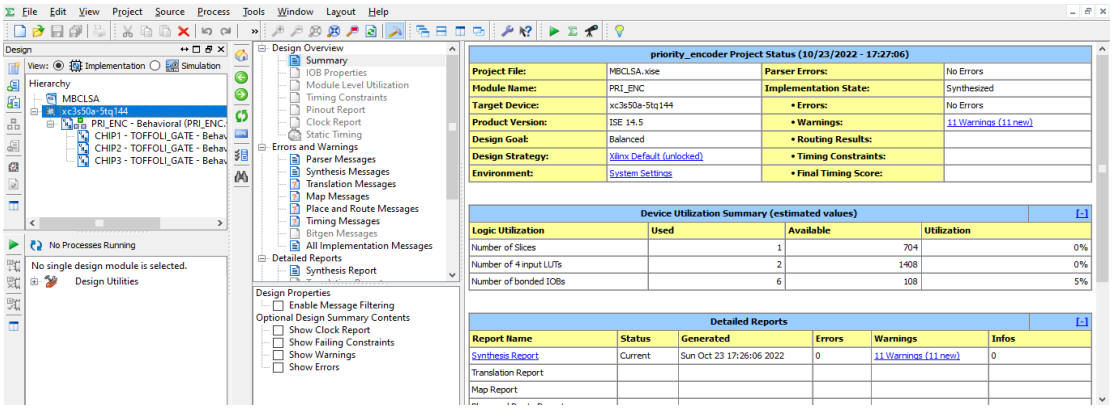

Figure 9. Device Utilization of Proposed 4:2 bit Reversible Priority encoder with Toffoli gate

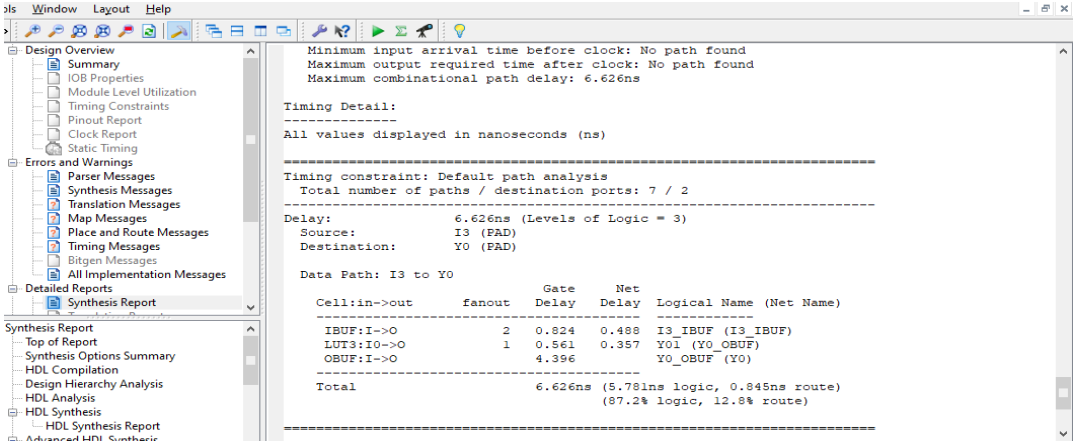

Figure 8. Timing summary of Proposed 4:2 bit Reversible Priority encoder with Toffoli gate

IV. CONCLUSION

One method to lessen the heating issues brought on by the increased component density on a single chip area is to develop reversible logic circuits. This encourages scientists to create reversible computers for conditions with preferably no power loss. This study proposes a simple, convertible 4 to 2 prioritized encoding design for the BCD platform.. The low-cost Toffoli gate design is suggested for use in reversible encoder circuit implementation. The suggested designs are assessed structurally using the BCD Developer simulation tool. The results reveal that we employed 15 TOFOLLl entries and 5 CNOT gates in this circuit, giving the circuit a total sharp rise of 80.

REFERENCES

1. Ramesh, G.P., Prabhu, S. (2021). FPGA Implementation of 3D NOC Using Anti-Hebbian for Multicast Routing Algorithm. In: Sharma, D.K., Son, L.H., Sharma, R., Cengiz, K. (eds) Micro-Electronics and Telecommunication Engineering. Lecture Notes in Networks and Systems, vol 179. Springer, Singapore. https://doi.org/10.1007/978-981-33-4687-1_29.
2. Chang, Y. J., and Huang, S. W. (2010, August). a comparator that uses a complete parallel priority encoder architecture. 53rd International Symposium Midwest Conference on Systems and Circuits took place in 2010 (pp. 877-880). IEEE.
3. Delgado-Frias, J. G., &Nyathi, J. (2000). A high-performance encoder with priority lookahead. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 47(9), 1390-1393.
4. Nguyen, X. T., Nguyen, H. T., & Pham, C. K. (2017). A scalable high-performance priority encoder using 1D-array to 2D-array conversion. IEEE Transactions on Circuits and Systems II: Express Briefs, 64(9), 1102-1106.
5. Harb, S., Abdel-Hafeez, S. (2006). a high-performance priority encoder on a VLSI that makes use of a common CMOS library. Express Briefs, During That on Devices and System II, 53(8), 597–601.
6. Gunasekaran, Ramesh, G.P. (2020). Design of Digital FIR Filters for Low Power Applications. In: Solanki, V., Hoang, M., Lu, Z., Pattnaik, P. (eds) Intelligent Computing in Engineering. Advances in Intelligent Systems and Computing, vol 1125. Springer, Singapore. https://doi.org/10.1007/978-981-15-2780-7_48Sakthivel, B., & Padma, A. (2020). Area and delay efficient GDI based accuracy configurable adder design. Microprocessors and Microsystems, 73, 102958.
7. De, D.; Das, J. C. (2019). New Toffoli gate and Feynman gate-based reversible priority encoder design for quantum dot cellular automata. 6882–6903 in The Journal of High performance computing, 75(10).
8. Bhattacharjee, A., Biswal, L., Mondal, K., and Rahman, H. (2020, March). Priority encoder circuit with fault-tolerant quantum implementation utilising Clifford+ t-group. ISDCS, the Global Workshop on Devices, Circuit and Systems, will take place in 2020. (pp. 1-6). IEEE.
9. Sriram, A. and K. Abikayal (2017). Reversible gate with encoding are used in the design of a reversible comparator.
10. Babu, H. M. H. and Lisa, N. J. (2014, July). Reduction of a 2n-to-n reversible quantum BCD priority encoder. 2014 IEEE/ACM World Symposium on Nanosize Architectures Proceedings (pp. 77-82).
11. Tiwari, R. K., Mishra, G. R., and Shukla, V. (2014, December). An unique method for creating reversible logic in a decimal to BCD encoder. 2014 saw the first-ever ICPCES (World Congress on Power, Control and Embedded Device) (pp. 1-5). IEEE.
12. Saha, P.; Thabah, S. D. (2020). Utilising Peres and Feynman gates, new reversible BCD encoder design strategies. 38–42. ICT Express, 6(1).
13. K. Ghosh, M. M. Haque, & S. Chakraborty (2016, April). Design of priority encoder and reversible ternary adder/subtractor circuits. 2016 saw the inaugural ICCSP (International Conference on Communications and Signal Processing) (pp. 1290-1295). IEEE.
14. Sendhilkumar Prasad, N.C., Ramesh, G.P. (2020). Analysis of Digital FIR Filter Using RLS and FT-RLS. In: Solanki, V., Hoang, M., Lu, Z., Pattnaik, P. (eds) Intelligent Computing in Engineering. Advances in Intelligent Systems and Computing, vol 1125. Springer, Singapore.

https://doi.org/10.1007/978-981-15-2780-7_63Chang, T. Y., and Chen, Y. H. (2011). a conditional-probability estimator with good adaptive accuracy for fixed-width Booth multipliers. 59(3), 594-603, IEEE Transactions on Circuits and Systems I: Regular Papers.