Original Article

Accuracy Configurable Adder Based On The Conventional Cla

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Doi: 10.47750/Pnr.2022.13.S02.313

Abstract

The speed and power consumption of a digital signal processing (DSP) system are directly related to the adder, an essential arithmetic module. Due to the requirements for high speed, power efficiency, approximate adders have been created. In error-tolerant applications like multimedia processing, machine learning, and many others, approximate computing is a potent technique for lowering energy consumption and computational delay. In these circumstances, designing effective digital data-paths is of utmost importance. The addition operation has therefore received a lot of attention. The majority of the earlier approximate adders, though, were made for Application Specific Integrated Circuits (ASICs), so it seems impossible to use them with other hardware, like Field Programmable Gate Arrays (FPGAs) (or at least ineffective). This paper describes a brand-new approximate addition method that makes use of an FPGA device's configurable resources. In this paper, anCarry maskable approximate adder without the cost of increased power consumption or delay for configurability was proposed. The conventional CLA serves as the foundation for the proposed adder, and runtime accuracy configuration is accomplished by masking carry propagation. In comparison to the traditional CLA, the proposed adder speeds up with a small area overhead, according to the experimental results.

Keyword:- Field Programmable Gate Arrays (FPGA), ripple carry adder (RCA), carry-lookahead adder (CLA), Accuracy configurable adder.

I. INTRODUCTION

The primary goals in the design of DSP units, especially compact devices, are increased speed and reduced power consumption. Speed is typically a trade-off between greater energy usage in the individual processing units and increased speed. One way to boost performance is to compromise computation accuracy [1]. Applications that can tolerate errors have been developed using this approximate computing strategy. Adder units, which make up the majority of the DSP system's arithmetic unit, consume a lot of power and frequently cause hotspots on the die [2].

An adder, a fundamental part of arithmetic operations, is frequently utilized in IC. A fixed accuracy design approach has been widely used in studies to create approximate adders. The accuracy of these adders, however, cannot be changed and they cannot be used to calculate precise values. Aside from that, despite their benefits like high performance and a small circuit area, approximate adders find it difficult to meet the various accuracy standards of various applications [3]. Adders are crucial parts of mathematical and logical systems (ALUs). Adders are among the most power-hungry parts of processors and frequently hotspot locations [4]. Adders are used to perform other operations like subtraction, multiplication, and division.

In accuracy customizable adders, the number of error levels is fixed. Depending on the control input, the adder's error varies. The most precise findings are produced at the highest level, while the most approximate results are produced at the lowest level. The proposed design occupies more space than the corresponding precise design since the design of such adders can produce both approximate and accurate outcomes. The proposed adder nevertheless conserves space in a larger sense since it does away with the necessity for two adders: approximate and exact [5]. For error-tolerant workloads, approximate computing is advantageous because it enables an exchange between precision and energy. In certain technology areas, this tradeoff is considerable at the time [6].

As one of the popular data operators in these applications, adders have attracted a lot of interest recently for their usage in approximation computing. The typical ripple carry adder (RCA) simply employs one adder of specified length to the inputs, making the carry chain the path that is most important [7].Devices that have recently evolved, such as picture identification and synthesis, computationally demanding DSP, and battery-powered wearable devices, have prompted concerns about power utilization. The basic arithmetic action of addition is used for these objectives. Minor error tolerance is already integrated into the majority of these applications. The revelation that addend settings control the actual worst-

case path delay is the cornerstone of the self-configuration idea. The real route delay doesn't become noticeable until a carry is transmitted over a number of successive bits.By utilizing the inherent tolerance characteristic, exact performancecan be used to find a compromise between precision and power [14].
This paper describes a brand-new approximate addition method that makes use of an FPGA device's configurable resources. The conventional CLA serves as the foundation for the proposed adder, and runtime accuracy configuration is accomplished by masking carry propagation. In comparison to the traditional CLA, the proposed adder speeds up with a small area overhead, according to the experimental results.

II. LITERATURE WORKS

Wenbin Xu et al. [8] proposed a SARA layout It has a significantly lower power/EDP than the most other methods. Additionally, compared to nearly all earlier works, SARA has a substantially smaller area overhead. The precision efficiency is even higher when using a DAR technique. Using multiplication circuits and DCT computing circuits, they show the effectiveness of our adder in image processing.

AyadDalloo et al. [9] The generalization of amethod for approximate adders results in the proposal of an ideal approximate adder. When compared to the some other methodit is a best method. Utilizing mathematical analysis and experimental data,it has been shown that OLOCA is superior to the current approximate adders.

Jin Miao et al. [10] a theoretical strategy for approximating adder analysis and synthesis We formally demonstrate the existence of optimal AFIC adder structures using our method, which uses regular, aligned carry adds to achieve larger significance bits. They also demonstrated that a wide range of design options with various quality-energy tradeoffs may be synthesized within the domain of AFIC adders. This covers approximation versions for use in diverse application requirements, whether they exhibit overestimating, underestimating, or dithering behavior. A total energy reduction of more than 40% is achieved by incorporating the suggested approximate adders into practical image processing architectures while maintaining excellent image quality.

Qian Wang et al. [11] demonstrated a concurrent liquid state machine core tech on an FPGA that uses power gating based on firing activity and arithmetic computation with executable extendable accuracy to significantly save energy for a language processing standard without significantly affecting recognition accuracy. They address a range of important design issues in their work, including reservoir connections and arithmetic block design.

Raunaq Nayar et al. [12] A novel approximation adder called HOAANED was introduced. It has a error distribution, an optimized RMSE, and almost no AE. In terms of design metrics, HOAANED is equivalent to other approximation adders based on physical realization. Using a program for processing images, HOAANED has been used to show the worth of the technology by outperforming its rivals in terms of PSNR.

Andrew B. Kahng et al. [13] proposed an ACA adder that allows for on-the-fly adjustments to the results' correctness. The ACA adder can provide up to a 24.6% throughput improvement and a 37.0% power savings over the conventional CLA adder. It also offers high metric precision. Applications for precisely customizable pipelining can also use the ACA adder. They demonstrate that when compared to a typical pipelined adder, it produce power reduction. Finally, we show how, given certain accuracy restrictions, their ACA can increase the potential quality, and power tradeoff.

Tongxin Yang et al. [14] developed an adder with adjustable precision without increasing power consumption or processing time. By masking the carry propagation, the indicated adder's runtime precision modifications can be achieved. It is based on the standard CLA. The results obtained show that the suggested adder works better than the traditional CLA in terms of speed and energy savings while occupying less space. When related to previously analyzed configurable adders, the testing findings further show that the proposed adder meets the stated goal of providing an objective optimum result between power and latency without compromising performance. The assessed application's quality standards were likewise found to be unaffected.
Summary:

- Currently used adder OLOCA exhibits less improvement in both error and hardware cost measures than the proposed adder.
- Utilizing mathematical analysis and experimental data,it has been shown that OLOCA is superior to the proposed approximate adders.
- It makes use of the discrepancy between the accuracy level required by devices and the accuracy provided by the computer device to achieve a number of enhancements.

III. PROPOSED METHOD

This research suggested an adder that may be configured for precision without costing more power or adding delay. The recommended adder is built on the CLA, and runtime precision adjustments can be made by masking the carry propagation. According to the testing findings, the recommended adder outperforms the conventional CLA in terms of speed and power savings while using less overhead space.

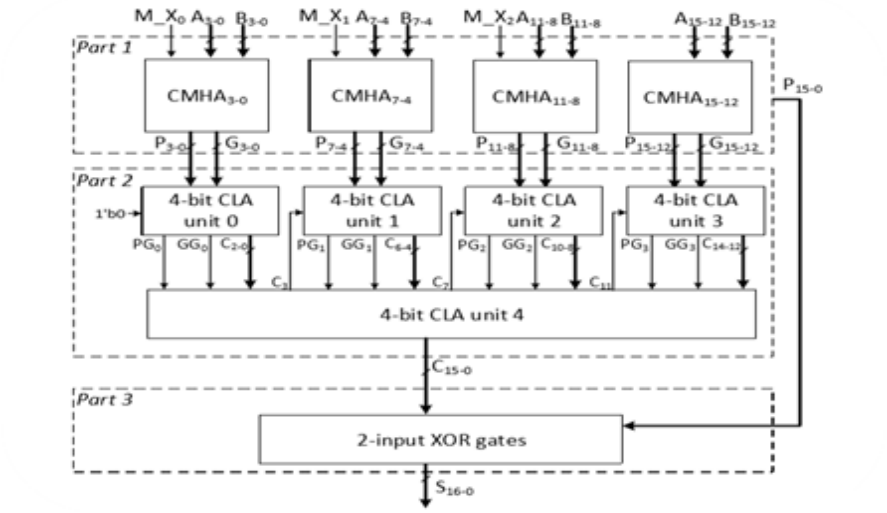

Figure1. Circuit Diagram

i)Carry Look Ahead Adder

CLA method employs the technique of generating carry bits all at a time to reduce delay. If we denote S as sum, C as carry, and A, B as the input bits, then sum and carry bit using CLA method.

$$P_i = A_i \oplus B_i,\ G_i = A_i . B_i \qquad (1)$$

$$C_i = G_i + P_i . C_{i-1} \qquad (2)$$

$$S_i = P_i \oplus C_{i-1}, \qquad (3)$$

Complete schematic of the of carry-out bit C4 including the AND gates and the XOR gates is represented by Fig. 1.

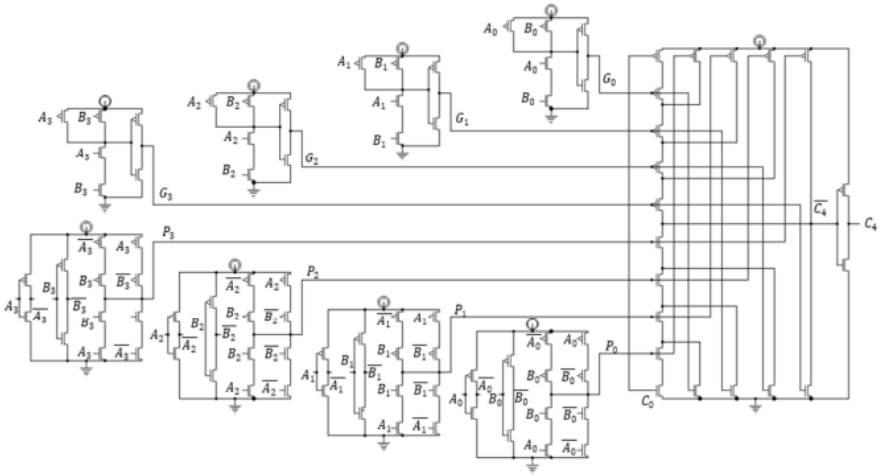

Figure2. Conventional design of carry-out bit C4.

Half adders prepare the signal for carry generation (G) and propagation (P), carry look-ahead units perform the carry generation, and XOR gates perform the sum generation. These three components make up a standard CLA. The primary focus of Part 1 is on half adders for G and P signal preparation. Think about an n-bit CLA, where each component may be produced as follows:

$$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0 \qquad (5)$$

Where

$$C_0 = \text{input carry bit}$$
$$C_4 = \text{output carry bit}$$

Where I denotes the bit position beginning with the least important bit. Pi is defined here as Ai XOR Bi rather than Ai OR Bi since the Ai XOR Bi circuit is utilized for Si generation. Since C0 and G0 are equivalent, if G0 is zero, then so is C0 [13]. From (2), we can infer that C1 = G1 when C0 is 0.

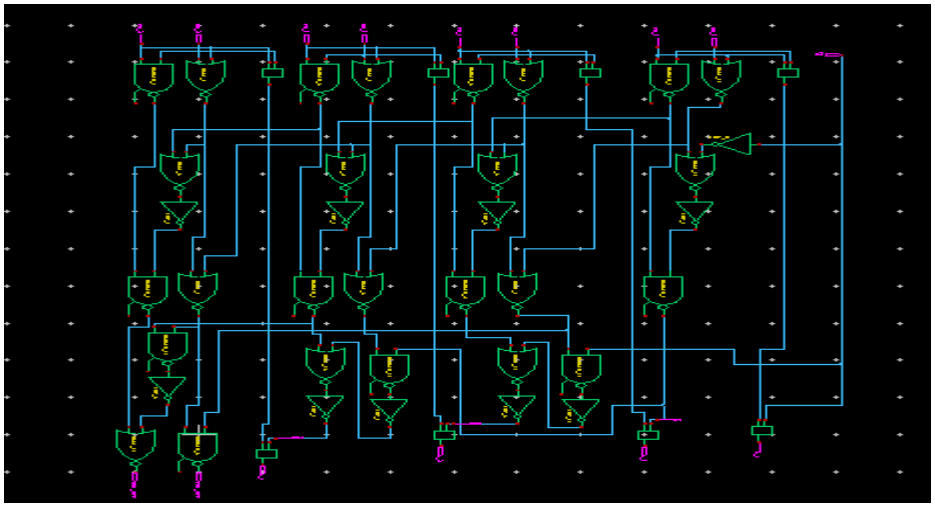

Figure3. 6-bit Carry look ahead adder

ii) CMA – Carry Maskable Adder

A conventional half adder is shown in Fig. 2(a). A 2- input XOR gate is used to generate sum s and a 2-input AND gate is used to generate carry Cout. An equivalent circuit of a half adder is shown in Fig. 2(b). The dashed frame represents an equivalent circuit of a 2-input XOR gate. Since there is a 2-input NAND gate in the dashed frame, we reuse it and add an INV gate to generate the carry signal Cout. The outputs of the 2-input NAND and OR gates in the dashed frame are named u and w, respectively. Table 1 is the truth table for the equivalent circuit of a half adder.

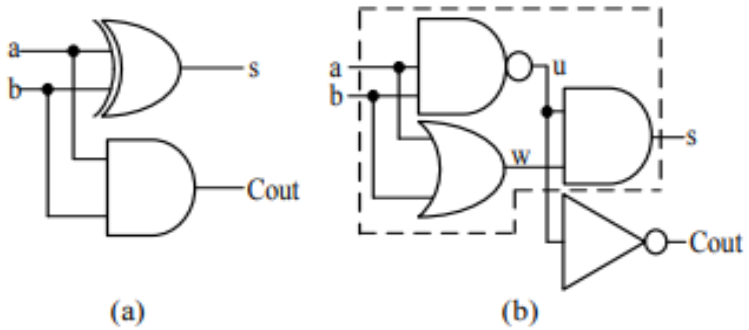

Figure4. (a) Conventional half adder, and (b) equivalent circuit of a half adder.

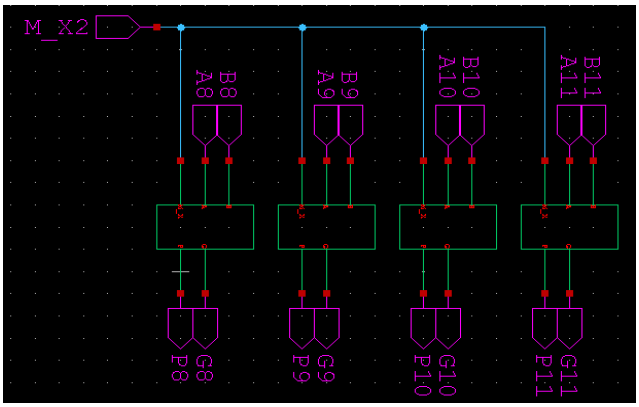

Figure5. 4-bit carry maskable adder

iii) Approximate configurable adder

Previous approximate adders struggled to locate and correct errors since they were designed for applications with a target precision and error-acceptable requirements. However, depending on the application, accurate calculations are occasionally still needed. Although VLSA can produce precise results, error identification and repair have a considerable time and space overhead [12]. To achieve the power-delay tradeoff, different precision settings or varying supply voltages might be employed. Different setting and voltage combinations could produce an excessive amount of results that are challenging to comprehend, especially when accuracy is needed [7].

The suggested approximate adder implementation can be made more widespread. The (N/k1) submodules listed in Equation 4 make up the approximation adder.

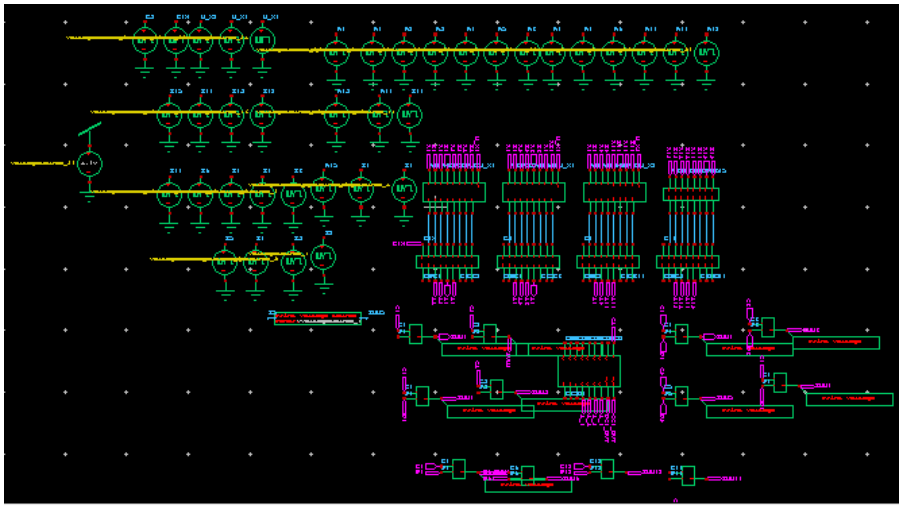

Figure6. Tanner design of proposed approximate adder

$$SUM[N - ik - 1 : N - (i + 1)k] = A[N - ik - 1 : N - (i + 2)k] + B[N - ik - 1 : N - (i + 2)k], \quad where\ i = 0, \ldots, N/k - 2 \qquad (4)$$

Since Cdelay and Carea are constants for delay and area, respectively, the critical path delay can be expressed using Equation (5) and the estimated area by Equation (7).

$$delay = Cdelay(log2k + 1) \qquad (5)$$

$$area = Carea(N - 2k)(log2k + 1) \qquad (6)$$

$$Power_{dyn} = Cpower(N - 2k)(log2k + 1)^2 \qquad (7)$$

The energy of the ACA can be roughly calculated as follows. With voltage scaling and a constant capacitance, dynamic and frequency power consumption are inversely correlated. Using both static and dynamic power, Synopsys Prime Time calculates power dissipation.

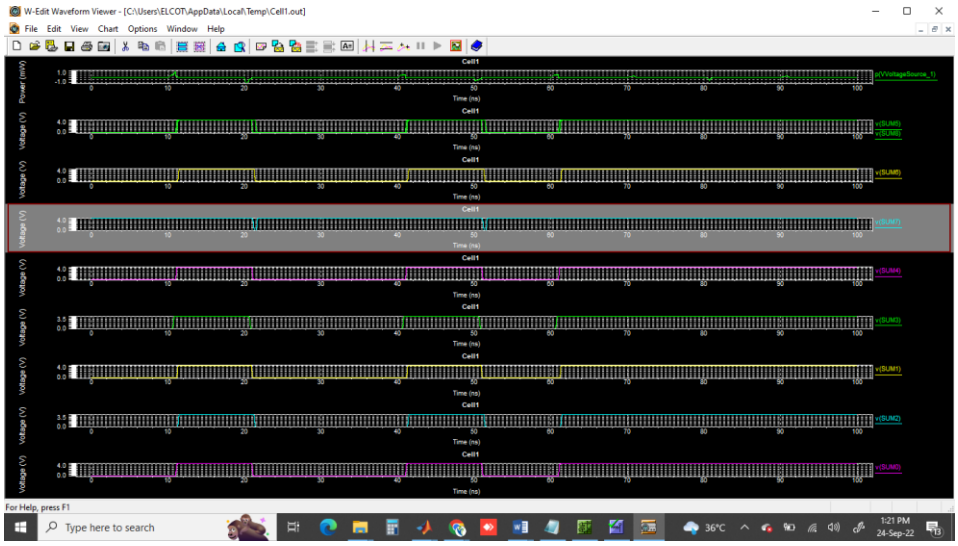

Figure6. Output Waveform of Proposed Adder

Table-I Power, Delay, PDP and error comparison

	Power(mV)	Delay(ms)	PDP(uJ)	Error rate(%)
GLSA	17.824	1.763	19.587	23.5
CCAA	14.335	1.323	18.965	12.7
ACAA	10.24	1.155	11.827	6.5
CMAA	8.563	1.126	9.642	2.7

GSLA- Gate level Static Approximate adder
CCAA- consistent carry approximate adder
ACAA - accuracy-configurable approximate adder

CMAA – Carry mask approximate adder

Figure7. (a) Power (b) Delay (c) PDP and (d) Error rate comparison on different addders

Above a, b c and d represents power, delay, Power delay profile and error rate of four different approximate adders. Here we can see on all 4 parameters our proposed approximate adder designed with carry maskable adder incorporated in CLA performs best. With GSLA show lowest performance. Error rate on addition result have been reduced a lot.

IV. CONCLUSION

It was proposed to employ a reconfigurable approximation carry look-ahead adder that operates at high speed while consuming little energy. The adder was suitable for both error-tolerant and precision applications because of its adaptability to switch between approximate and accurate operation modes. The proposed adder's structure was based on certain modifications to the standard CLA structure where CLA is designed with Carry maskable half adder. In this paper, a reconfigurable approximation CLA for high-speed applications is proposed. In this paper, an ACAwas proposed without incurring the expense of increased delay or power for configurability. The suggested adder is based on the traditional CLA, and its accuracy may be modified at runtime by masking the carry propagation. It has significantly improved both error and hardware cost metrics in biomedical sensor devices [15]. The final result show that the suggested adder saves significant power and speeds up with a little area overhead compared to the standard CLA.The proposed CMAA shows 60% improvement on error rate.

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