# Comparitive Study of Single, Double and Multi Shell CNTMOSFET for Biosensing Applications

**P. Geetha[1], Hirald Dwaraka Praveena[2], Katta Sudha[3]**

[1]Professor, Department of ECE, School of Engineering and Technology, Mohan Babu University, Tirupati, A.P, India.

E-mail: mailpgeetha2013@gmail.com

[2]Assistant Professor, Department of ECE, School of Engineering and Technology, Mohan Babu University, Tirupati, A.P, India.

E-mail: hdpraveena@gmail.com

[3]Assistant Professor, Department of ECE, Sree Vidyanikethan Engineering College, Tirupati, A.P, India.

E-mail: sudhak.ece@gmail.com

## Abstract

It becomes very significance to sense and quantify the proteins in the fields of biotechnology. Among various other nano bio sensors, carbon based devices serves well in effective sensing applications. The sensed data can be quantified using a CNT based MOSFET. Carbon Nano Tube consists of multi shells, one inside another, contributes good conductance compared to Single-walled Carbon Nano. Each shell can have different chiralities depending on the direction they are rolled up and multiwalled are always metallic. Modelling and performance analysis of Multi-walled Carbon Nano Tube based devices are addressed less due to their complexity in both structure and characterization. In this paper, Multi-walled Carbon Nano Tube Field Effect Transistor is analytically modelled and simulated to study its electric performance characteristics with respect to Single, Double shells based samae device. Various device parameters viz., gate dielectric (k1), gate distance from the channel (h), number of channels(N), gate length(Lg) are varied, plotted and the corresponding capacitance responses are compared.

**Keywords:** Multi-walled Carbon Nano Tube, Dielectric Strength, Gate Length, Number of Channels, Drive Capacitance.

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## INTRODUCTION

The unique nature of Carbon Nano Tubes supports to perform better than the conventional device if placed as an array of parallel channels. Also, the graphene sheet is folded to form either single or multi-layers resulting in single-shelled or multi-shelled Carbon Nano Tubes. Device containing multi-shelled channel is preferred over single- shelled device since, the former provides high ON- current and manages the signal delay. The shells other wise are called as walls in this paper.

CNTFET and CNT interconnect has been modelled using Verilog-A hardware description language[1].

To describe the intrinsic current–voltage and charge–voltage characteristics [2] proposed a data-calibrated compact model of carbon nanotube (CNT) FETs (CNTFETs) based on the virtual source (VS) approach. Compact modeling based on the Landauer formula for ballistic transport in the CNTs is one of the effective method for assessing the performance. [3] & [4]. To simulate the quantum transport in CNTFETs and to assess its performance, Non equilibrium Green's function (NEGF) formalism [5] - [8] & [13] has been extensively employed.

The authors (Ado Jorio et al 2007) [9] of the book reviewed details regarding the structure of CNTs along with electrical, optical, transport properties of Single and Multi-Wall CNTs. It was stressed that with easier synthesis, MWCNT possesses high electrical and transport properties compared to that of SWCNT.

Kaihui Liu et al [10] (2008) claimed that the advantages of double-walled CNTs were stronger than single-walled CNTs with their unique mechanical, thermal and structural properties. In general, multi-wall CNTs during fabrication introduce alternative electrical properties to the individual walls (i.e. Metallic (M)/semiconducting(S), S/M, M/S, M/M). The paper tested these combinations and found that in DWCNTs of M/M and M/S combination there was no gate voltage modulation and in S/M DWCNTs the drain current was suppressed by gate voltage. S/S combination of DWCNTs was found to provide typical p-type semiconducting properties with ($I_{on}/I_{off}$) ratio as high as 104.

The advantage of co-axially gated device over the dual-gate is that the former provides aggressive scaling down of channel length. The intrinsic advantage of gate all around transistor is said to be more due to high mobility and ultrathin body. It allows the most aggressive gate length scaling with good channel control. The metal gate is wrapped around the channel.

Benjamin Iniguez et al (2007) [11] proposed a compact model using 1-D Poisson's equation in the perpendicular direction of channel length for Multiple-Gate MOSFET. As scaling down of device dimension faces difficulties, the multi-gate structures proved to be a right solution for their good channel control that in turn reduces the short channel effects and a

steep sub threshold swing. The noise and high-frequency performance were also been studied.

Bastien COUSIN et al [12] (2009) in their compact model for Gate-all around Si- nanowire transistor analysed the quantum-mechanical effects. The new device CMOS structure is needed for handling the problems of device downscaling process and multi-gate relevantly provide the solution[17]. The gate- all around structured transistor among the rest gives enhanced gate control to manage the short channel effect[18].

In this paper, a compact analytical model is used for the studying various characteristics of the device and the parameters are quantified. The complication in using multi-walls and multi-channels lies in computing the interferences caused by the adjacent channels as well as walls of the same channel. The screening and or imaging effects due to neighbouring channels and inter wall interference are included in this model. Three main capacitances are modelled for the devices containing single and double-walled channel. The equations for charges of individual channels and walls are solved self-consistently to get the device surface potential. It is followed by the calculation of substrate capacitances and driven capacitance. Driven capacitance is derived using the values of surface potential.

## Structure and Modelling of the Device

The key capacitors that are modelled are:

- The capacitance between gate and channel (Cgc)
- The fringe capacitance (Cof)
- The gate-to-gate capacitance or capacitance between gate and source or drain (Cgtg).

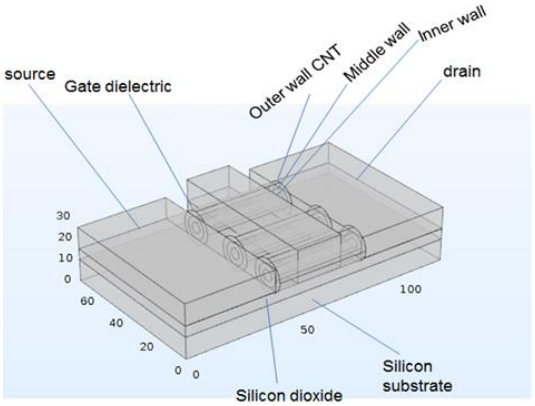


Figure 2.1a: Structure of the device

### A.Gate to channel capacitance (Cgc)

Cgc plays a significant role in determining the drive current of the device. The screening effects of neighboring parallel cylinders and imaging effects of individual walls are taken for consideration for modellingCgc [12]. In addition to the potential difference caused by the individual cylinders there is potential difference due to screening effects of neighboring cylinders.

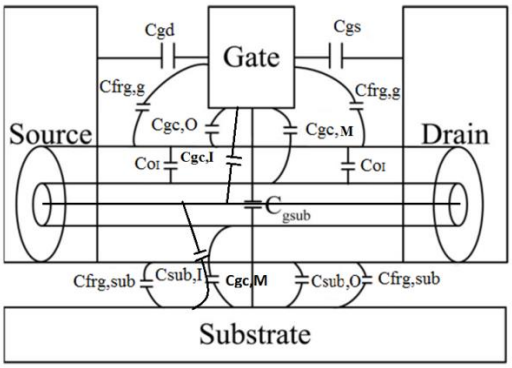


**Figure 2.1b.** Distribution of the capacitances

Gate to channel capacitance (Cgc) of MWCNT is of three parts, i.e. Capacitance between

Gate and outer wall of the channel (Cgc, o) and

Gate and inner wall of the channel (Cgc, i)

Gate and middle wall of the channel (Cgc, m)

Cgc, o is calculated as in [9] and also in [15] & [16].

$$C_{gc,o} = \frac{1}{\frac{1}{Cgc,o^{(o)(o)}} + \frac{1}{Cgc,o^{(o)(m)}}} \quad (1)$$

Where, Cgc, o(o)(o) - Gate channel capacitance of the outer wall and the screening effects of other MWCNT.

Cgc, o(o)(m) - Gate channel capacitance due to screening effects of the middle wall.

Cgc(o)(o) is further divided into Cgc,e(o)(o) and Cgc,m(o)(o).The first case is for the channels at end of the array and the second is for the middle ones. Cgc,e(o)(o) is effected by the neighboring channel at one side alone whereas Cgc,m(o)(o) is effected by channels at both the sides. They are calculated from [11] & [12].

$$Cgc,o^{(o)(o)} = \begin{cases} Cgc,e^{(o)(o)} = \frac{Cgc,inf.Cgc,sr}{Cgc,inf+Cgc,sr} \\ Cgc,m^{(o)(o)} = 2.Cgc,e^{(o)(o)} - Cgc,inf \end{cases} \quad (2)$$

Where, Cgc, inf - gate channel (outer wall) capacitance without any screening effects.

Cgc, sr - the equivalent capacitance including the screening effects of the other channels in the array.

Cgc, inf is calculated as in for cylindrical GWA CNTFET,

$$Cgc,inf = \frac{2\pi\kappa_1\varepsilon_0}{cosh^{-1}\left(\frac{2h}{d_o}\right)+\frac{1}{3}\lambda_1 ln\left(\frac{2h+2d_o}{3d_o}\right)} \quad (3)$$

where,

λ1 - is the pre-factor that accounts for the interface of dielectrics κ1 and κ2 with different values, calculated as in [3(a)]. The above equation is similar to the planar gate [15] & [16], the term $\frac{1}{3}$ stands for gate all around transistors.

$$\lambda_1 = \frac{\kappa_1-\kappa_2}{\kappa_1+\kappa_2} \qquad 3\ (a)$$

Cgc, sr is estimated by takinga. The potential drop between gate and outer wall and b. The potential drop due to the screening effects of the double walls of the neighbouring

TWCNT [21-22].

$$\mathrm{Cgc,sr} = \frac{1}{\frac{1}{\mathrm{Cgc,sr^{(o)(o)}}}+\frac{1}{\mathrm{Cgc,sr^{(o)(I)}}}} \quad (4)$$

$$\text{where,}\mathrm{Cgc,sr^{(o)(o)}} = \frac{4\pi\kappa_1\varepsilon_0}{\ln\left(\frac{s^2+2(h-r_o).\left[h+\sqrt{h^2-r_o^2}\right]}{s^2+2(h-r_o).\left[h-\sqrt{h^2-r_o^2}\right]}\right)+\ln\left(\frac{s^2+2(h-r_o).\left[h+\sqrt{h^2-r_o^2}\right]}{s^2+2(h-r_o).\left[h-\sqrt{h^2-r_o^2}\right]}\right)+\lambda_1\ln\left(\frac{(h+d_o)^2+s^2}{9r_o^2+s^2}\right).\tanh\left(\frac{h+r_o}{s-d_o}\right)} \quad (5)$$

Where,

s is the pitch distance between the array of the multi walled CNT's.

h is the distance of the gate form the channel.

k1 is the gate dielectric constant used i.e., hafnium oxide whose k1=16.

$$\text{Here, } \mathrm{Cgc,o^{(o)(I)}} = \frac{Q_A^{(o)}}{Q_A^{(I)}}\,\mathrm{Cgc,inf} \quad (6)$$

To find out Gate and inner wall of the channel (Cgc, I) [20], [21] & [22],which comprises of

The effects of inhomogeneous gate dielectric and the imaging effects of other neighbouring GWAMWCNT.

The imaging effects of the outer wall.

$$\mathrm{Cgc,I} = \frac{1}{\frac{1}{\mathrm{Cgc,o^{(I)(o)}}}+\frac{1}{\mathrm{Cgc,o^{(I)(I)}}}} (7)$$

$$\mathrm{Cgc,I^{(I)(o)}} = \frac{Q_A^{(I)(o)}}{Q_A^{(o)}}\,\mathrm{Cgc,o} \quad (8)$$

$$\mathrm{Cgc,I^{(2)(2)}} = \frac{2\pi\varepsilon_0}{\ln\left(\frac{d_o}{d_I}\right)} \quad (9)$$

where, do and are $d_I$ diameters of the cylinder, is Lattice Constant( 2.49A°)

Cgc, m- which is the gate to channel capacitance due to the middle wall can be found with the help of the equation below

$$\mathrm{Cgc,m} = \frac{1}{\frac{1}{\mathrm{Cgc,o^{(m),(o)}}}+\frac{1}{\mathrm{Cgc,o^{(i),(m)}}}+\frac{1}{\mathrm{Cgc,o^{(m),(m)}}}} \quad (9a)$$

The gate to channel capacitance on the outer wall with respect to the middle layer can be found from the equation below

$$\mathrm{Cgc,o^{(o),(m)}} = \frac{Q_A^{(m)}}{Q_A^{(o)}}\mathrm{Cgc,o} \quad (9b)$$

The gate to channel capacitance on the middle wall with respect to the inner wall can be deteremined by the following equation

$$\mathrm{Cgc,o^{(m),(i)}} = \frac{Q_A^{(i)}}{Q_A^{(m)}}\mathrm{Cgc,o} \quad (9c)$$

$$\mathrm{Cgc,o^{(m),(m)}} = \frac{2\Pi\varepsilon_o}{\ln\frac{d_o}{d_m}}\mathrm{Cgc,o} (9d)$$

## B. Fringe Capacitance (Cof)

The capacitance between gate and source (Cgs), the capacitance between gate and drain (Cgd), the capacitance between gate and the channel (Cfrg,g), capacitance between the substrate and channel (Cfrg,sub) are classified as Fringing capacitance. Being a strong function of device geometry, importance of fringing capacitance lies in evaluating the device speed accurately [20], [21] & [22]. The outer fringing capacitance (Cof) alone is considered here and other fringes are out of scope of the work. Cof is assumed to be independent of Hgate and divided into two categories. One at the ends Cof, e and the other at the middle *Cof,m* same way as the method followed to do *Cgc*.

For wrap around gate FET,

$$\mathrm{Cof,m} = \frac{2\alpha}{\eta_1}\,\mathrm{Cof,e} + \left(\frac{1-2\alpha}{\eta_1}\right).\left(\frac{\pi\kappa_2\varepsilon_0 \mathrm{Lsd}}{1/3\,\cosh^{-1}\left(\frac{(4h^2)+(0.56\mathrm{Lsd})^2}{d_o}\right)}\right) (10)$$

Where,

$$\alpha = \exp\left(\frac{N-3}{\tau_2 N}\right), N \geq 3 \quad (10a)$$

$$Cof,e = \frac{\pi\kappa_2\varepsilon_0 Lsd}{ln\left(\frac{(4h^2)+(0.56Lsd)^2+s^2}{s}\right)+ln\left(\frac{\sqrt{(s/2)^2}}{2}\right)+exp\left(\frac{\sqrt{Na^2-2N}+N-2}{\tau_1 N}\right)\ \frac{1}{3}cosh^{-1}\left(\frac{(4h^2)+(0.56Lsd)^2}{d_o}\right)}, N \geq 2 \quad (11)$$

$\boldsymbol{\tau_1,\tau_2}$ are fitting parameters describing the rate of decrement in electric flux of the neighbouring cylinders with increase in distance between them. $\tau_1,\tau_2$ are taken as 2.5 and 2.0 respectively from [17].

## C. The gate-to-gate (or gate-to-S/D) coupling capacitance (Cgtg)

Cgtgis one more main capacitance and it can be separated into

2.3.1. Gate-to-gate fringe capacitance per unit length Cgtg,fr

2.3.2 Gate-to-gate plate capacitance per unit length Cgtg,nr due to normal electric field between the two channels.

Cgtgis the summation of both Gate-to-gate fringe capacitance per unit length Cgtg,fr and Gate-to-gate plate capacitance per unit length Cgtg,nr[20].

$$\mathrm{C_{gtg}} = \frac{3\kappa_2\varepsilon_0 \mathrm{H_{gate}}}{\mathrm{Lsd}} + \alpha_{\mathrm{gtg,sr}}\frac{\pi\kappa_2\varepsilon_0}{\ln\left(\frac{2\pi(\mathrm{Lsd}+\mathrm{Lg})}{2\mathrm{Lg}+\tau_{\mathrm{bk}}\left(\mathrm{H_{gate}}+\mathrm{h}+\mathrm{r_O}\right)}\right)} (12)$$

αgtg is the factor due to screening effect of neighbouring conductors(Gate/Source/Drain)

(αgtg = 0.7 for Hadj =Hgate)

where,

$$\tau_{\mathrm{bk}} = \exp\left(\frac{\left(2-2\sqrt{1+2}(\mathrm{H_{gate}}+\mathrm{Lg})\right)}{\mathrm{Lsd}}\right), (13)$$

The drive capacitance is calculated using the following relation [13],

$$C = \boldsymbol{C_g L_g + f_{miller}.2\left(C_{of}^{(g)} L_s + C_{gtg} W_{pitch}\right) + C_{gsub}} \quad (14)$$

where, fmiller =1.5. (constant from the reference)

Ls is the length of the source

Cgtg is the gate to gate fringe capacitance per unit length

Cgsub is the gate to substrate capacitance.

The enhanced performance characteristics of the triple walled wrap around gate carbon nano tube field effect transistor against the double walled CNTFET in terms of many characteristics is achieved.

As the number of channels is increased then the performance of the device also increases. It is checked for many number of channels and their capacitances. The parameters like the gate

length and pitch distance (the distance between the two cylinders of graphite sheets) can also be varied and the performance of the device can be predicted.

The graphs for all the single walled, double walled, and triple walled (multi walled) are plotted such that the variation among them can be known.

The materials used for the device is three carbon nano tubes, silicon dioxide as a insulator, silicon is used for source and drain contacts and hafnium oxide is taken as gate dielectric because it has the highest dielectric constant 16 when compared to the others. The high k value gives the high performance.

## Results and Discussions

A multi-walled gate wrap around array carbon nanotube field effect transistor (MWGWA CNTFET) is analytically modelled; the corresponding results are simulated and plotted for study. The parameters involved in the modelling of the device are tabulated in Table 1.1. The parameters taken for study are gate dielectric (k1), the normal distance of gate from the centre of the channel(h) in nm, Number of channels (N), Gate length(Lg) in nm. The behaviour of the drive capacitance is studied by varying the k1 from 1 to 30; forh=5nm, 16nm, 20nm, 24nm, 30nm; for N=3, 5, 11, 15, 21; and Lg from 32nm to 61nm.It is observed that in all the cases multi-walled device excel in its performance when compared to its counter parts. The observations and inferences from the curves are stated individually for further study.

Table I

| Details of Parametric Values | | |
|---|---|---|
| ***S. No*** | ***Parameters*** | ***Values*** |
| 1. | CNT Diameter (do, dm, dI) | 2.4nm, 2nm,1.34nm |
| 2. | No. of CNTs | 3 |
| 3. | Oxide Thickness (Tox) | 4nm |
| 4. | Gate Dielectric | 16 |
| 5. | Power Supply | 0.9V |
| 6. | Gate/Source/Drain (Lsd) | 32nm |
| 7. | Gate Height (Hgate) | 12nm |
| 8. | Normal distance of gate from the channel (h) | 5nm |
| 9. | Pitch distance(s) | 20nm |
| 10. | Bulk dielectric Thickness(Hsub) | 10μm |
| 11. | Bulk dielectric Value(κ2) | 4 |
| 12. | Flat Band Voltage | 0V |
| 13. | n11, n12 | 35,0 |
| 14. | n22,n23 | 26,0 |
| 15. | n32, n33 | 17,0 |
| 16. | Lattice Constant(a) | 2.49A° |

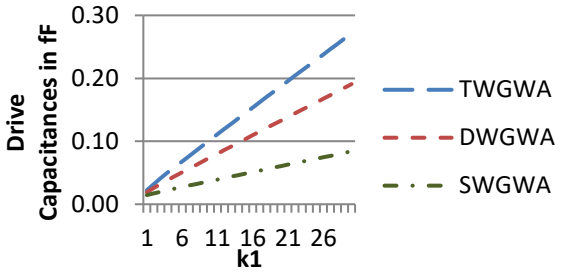


**Figure 3.1.** Illustration of response of Drive Capacitance with respect to k1

The above figure 3.1 depicts the variation of drive capacitance with respect to gate dielectric k1. The values of gate dielectric varies from 1 to 30. The response of the drive capacitance varies from 0.01 to 0.27 fF for TWGWA,. 01 to 0.19fF for DWGWA and 0.01 to 0.08 for SWGWA. The gate dielectric value 16 gives the drive capacitance as 0.16fF for TWGWA, 0.11fF for DWGWA and 0.05fF for SWGWA. So, it is inferred that the drive capacitance is increasing with increase in number of walls of the CNT that will lead to increase the flow of current through the channel CNTs.

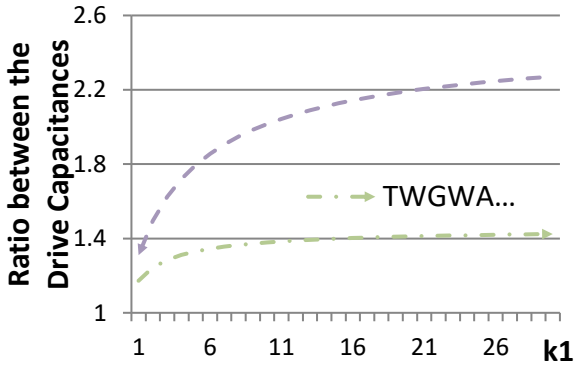


**Figure 3.2.** Illustration of performance improvement of drive capacitance for TWDWGA over DWGWA and that of DWGWA over SWGWA

TheFigure3.2 provides the performance improvement of TWDWGA over DWGWA and that of DWGWA over SWGWA. The ratio which the performance differs is calculated and plotted for study. It is found the improvement is 2.14 for DWGWA over SWGWA and 1.4 for TWGWA over DWGWA at k1=16. It is observed that

a) The curve for TWGWA over DWGWA increase exponentially from 1.17 at k1=1 to 1.3 at k1=9 approximated to constant.
b) The curve for DWGWA over SWGWA increase exponentially from 1.3 at k1=1 to 1.98 at k1=9 and variation after k1=16 slows down.

Thus, the inference from the graph is that

a) The drive capacitance gets improved as k1 is being increased and the improvement is more for DA Vs SWGWA than TWGWA Vs DWGWA.

In the figure3.3 depicts the behaviour of drive capacitance

against the variation of gate dielectric for different values of number of channels It becomes an important study with variation of number of channels, since during scaling downthe size of the transistor; the performance should be comparable with that of bulk devices. Also, during fabrication it is obvious that the process cannot be done with one or two number of channels because of the size of the nano size ofthe components. In this connection, the drive capacitance shows linear increments.

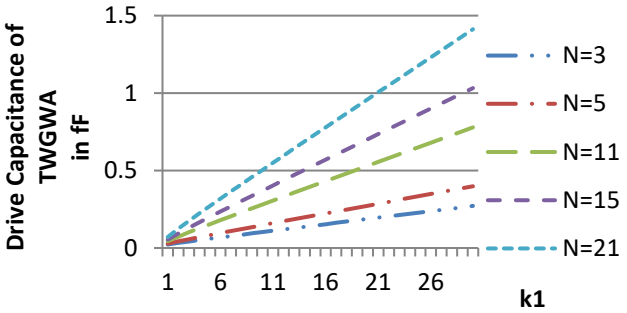


**Figure 3.3.** Illustration of variation of Drive capacitance(C) with respect to gate dielectric (k1) for various values of Number of channels.

Increase in number of channels. So, it can be inferred that the increase in number of channels favours the performance with respect to capacitance. The values of N=21,15,11,5 gives C= 0.778fF, 0.5699fF, 0.43fF, 0.223fF, 0.15373fF respectively at k1=16.

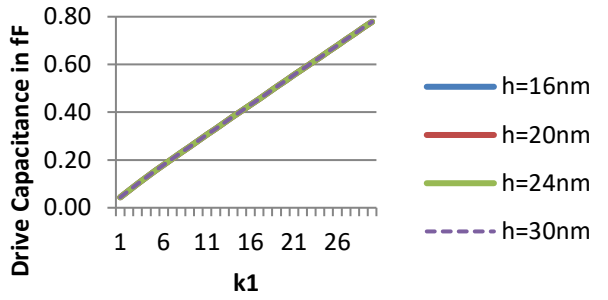


**Figure 3.4.** Illustration of variation of Drive Capacitance (C) with respect to gate dielectric (k1) for various 'h' distances.

The figure 3.4 shows the variation of Drive capacitance against the gate dielectric value for different 'h' distance in TWGWA, DWGWA and SWGWA. It is observed that the curve varies linearly for all the three cases. The variation starts with 0.04 fF and increases linearly till 0.75fF. So, it is inferred that the Drive capacitance shows same variation for TWGWA, DWGWA and SWGWA in value with respect to change in normal distance of gate from the channels for various gate dielectric strength.

The figure 3.5shows the variation of Csub against the gate dielectric value for TWGWA, DWGWA and SWGWA. It is observed that the curve varies linearly for all the three cases. The variation starts with 0.88 aF and increases linearly till1.67aF. So, it is inferred that the substrate capacitance does not show any variation with respect to change in number of walls of the channel for various gate dielectric strength.

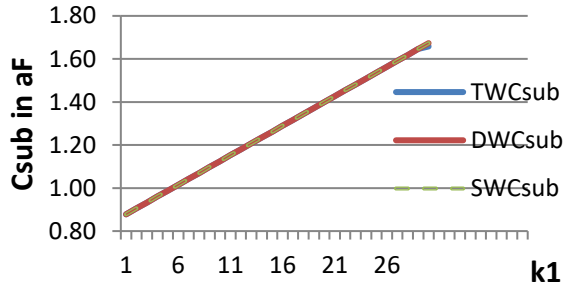


**Figure 3.5.** Illustration of variation of Substrate Capacitance (Csub) with respect to gate dielectric(k1)

## CONCLUSIONS

From the above study of drive capacitance for various device parameters, the following are the conclusions that have been arrived.

To increase the drive capacitance the number of walls of the CNT can be increased. The gate dielectric strength valuek1 can be increased and the improvement is more for DWGWA Vs SWGWA than TWGWA Vs DWGWA. The number of channels can be increased. The channel Gate length can be increased. In addition, it is found that the Drive capacitance shows same variation for TWGWA, DWGWA and SWGWA in value with respect to change in normal distance of gate from the channels for various gate dielectric strength. The substrate capacitance does not show any variation with respect to change in number of walls of the channel for various gate dielectric strength. Thus, this device design can be utilized to sense the biological components like proteins.

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