Original Article

Methodology for Hardware testing of an Application Specific Integrated Circuit (ASIC)

Navneet KaurBrar*[1], Manu Bansal[2],Alpana Agarwal[3]
Project Associate, Associate Professor, Professor & Head of Department
[1-3]Electronics and Communication Engineering Department
Thapar Institute of Engineering and Technology, Patiala, Punjab, India
navubrar1992@gmail.com[1], mbansal@thapar.edu2,alpana@thapar.edu
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Abstract

The paper demonstrates an efficient process flow for the Hardware Testing of an ASIC (Application Specific Integrated Circuit). The procedure is implied on Comparator, ADC (Analog-to-Digital) and Present Cipher Crypto ASIC. This involves the testing functionality of an Analog, Digital and Mixed Signal design ASIC. The results obtained during functional testing are verified through simulations on Cadence, in case of comparator and ADC ASIC, and vivado in case of Crypto ASIC. The method gives high accuracy and requires less power even at high frequency.

Index Terms: ASIC (Application Specific Integrated circuit), Filters, MSO (Mixed Signal Oscilloscope), FPGA (Field Programmable Gate Array)

I. INTODUCTION

ASIC (Application Specific Integrated Circuit) is an electronic IC (Integrated circuit) designed for a specific purpose that is reliable, requires less power, and provides greater performance, than an FPGA. Owing to its advantages ASIC are widely used in many sectors namely medical, transport, communication, defense and many more. The designing of an ASIC requires time and specialization, as it cannot be reprogrammed once manufactured. Therefore, before mass production the functionality of an ASIC should be tested. The challenge for testing of an ASIC is that not much indetail method or procedures are available to do Testing of an ASIC at hardware level. The paper proposes a methodology to test an ASIC of all domains which can be used for real time applications. Moreover, the results are validated through software simulations.

The manufacturing and design companies have issues application notes on testing of Analog, Mixed Signal Designs such as ADC, which has various usage in electronics [1]. However, digital design comparator ASIC Testing is hardly available. The cryptography chips is widely used in many domains, its functional testing of ASIC on software simulations [2] is accesible but not much could be found on Crypto ASIC hardware testing . The main contribution of the paper is as follows:

- The process flow is demonstrated for hardware testing of an ASIC of all designs that might vary same as per the ASIC domain and its operation.
- A detailed selection guide for peripheries of an ASIC such as Buffers, external filters for impedance matching to increase signal strength.
- The Grounding technique is demonstrated on basis of ASIC ring and core power supplies to reduce the coupling of noise i.e. generated in ASIC.
- The different methods to capture the output and give input signals are also demonstrated while testing the ASIC.

II. ASIC TESTING METHODOLOGY

The ASIC Testing contains two stages: Before and After PCB designing, demonstrated in Figure 1.

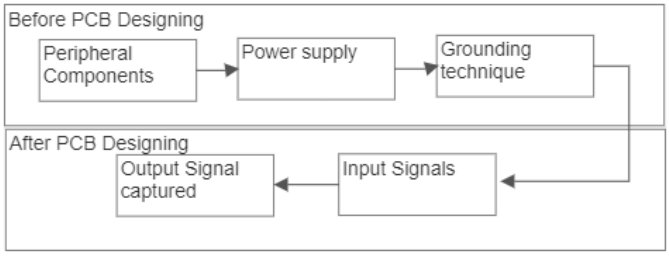


Fig. 1: ASIC Testing Methodology stages

A. Before PCB Designing

1) Peripheral Components: The components are required to interface the pins of an ASIC with the external world using peripheries to remove distortion while communicating. Some of them are buffers, resistance and capacitance to avoid cross coupling and noise distortions, whose choice is explained in detail as follows:

*a. Buffer***:** The buffer is an electronic circuit to segregate the input and output signal side and make sure the signal is not altered at the receiver side. It consumes very less current and does not distort the input circuit functionality. Moreover, it is used where signal requires high current gain while upholding the same voltage level of the signal. In digital circuits TTL buffers are not preferred as they have high input capacitance which leads to increase in dynamic switching currents, whereas CMOS buffer are used that operates around switching threshold voltages gives output as "0 or 1" as required in digital circuits **[q].** While choosing the buffers for the circuit one should make sure the saturation and delay time is less, lower power dissipation, high noise immunity and high output drive capability. The Figure 2. Shows the output with and without buffer [3]. The yellow output is of without buffer and pink one is of with buffer in which output is setlled in less time.

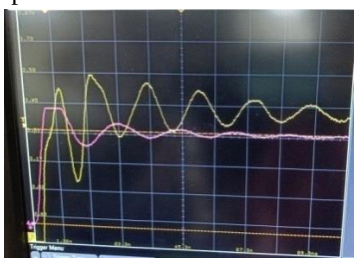


Fig.2. Transient Response Output with and without Buffer

b. Impedance Matching: The impedance matching is used to prevent signal reflections at the receiver side, provide maximum power transfer and make driver/receiver impedance resistive. The impedance matching circuit constitutes of filters of different types such as Pi, T, parallel LC and series/shunt. These filter behavior is usually High pass; low pass and band pass filters [4]. The rule of thumb while choosing resistor and capacitor values is that for high frequency circuits the capacitor and resistor value with lower values like 0.1 μF or 0.001 μF and 50Ω or 100 Ω respectively, vice versa for lower frequency signals.

c. Level Shifter: In electronic devices, the internal components are usually made of CMOS, as they are small in size and economic to use, which work at lower voltages. However, the external controllers or USB operate at 3.3 or 5V.Therefore, to communicate between ASIC and controllers a level shifter is required to convert data in to required voltages without altering the data.

d. Linear Dropout (LDO) Voltage Regulator: The power supplies available are usually of 5V, 9V or 12 V. But at commercial level lower voltage components are used in the circuit, as they are economic and libraries are easily available at software level of such components. Therefore, the designer uses LDO to drop the voltage and utilize the required level of voltage for the device.

2) Power supply: In an ASIC, there are number of power supply pins (VCC as VDD and Ground as VSS). This is to obtain efficient, signal integrity and power architecture. Moreover, some ASIC architecture requires multiple voltage values such as in microcontrollers. In some ASIC there are different analog and digital power supply pins. As some internal circuits need analog power supply like comparator, resistive ladder etcetera and digital power supply is requisite in encoders, gates etcetera. The multiple ground pins helps to provide more current path for the heat dissipation [5].

3) Grounding technique: The grounding plays an important role to test the circuit to prevent the unwanted noise, decoupling, corrupting performance especially in mixed signal devices and high speed circuits. In mixed signal designs, analog circuit and power supply is more susceptible to noise. Therefore, different power supplies for analog and digital power supplies should be used so as to hinder digital noise to distort the analog circuit functionality. Moreover, a 0.1µF capacitor ought to be used between VDD and VSS in high frequency circuits to remove unwanted noise and glitches from the power supply. The testing of an ASIC involves many electronic devices used; each device should be connected common ground in star configuration [5].

Once all the peripheral components, power supply and grounding technique is cleared, PCB is Designed.

B. After PCB Designing

1) Input Signals: The ASIC input signal includes the data, analog signal, clock, select signals and many more. The clock signal, digital data signal like any plain text could be given through controller or an FPGA. The analog and clock signal could be given from function generator as well. The select signal is just a controlled digital signal achieved through a switch interfaced with a controller, or an FPGA that has on-chip switch.

2) Output Signal captured: The output of an ASIC can be seen on an Oscilloscope weather be it analog or digital. The data displayed on oscilloscope can be saved in the pen drive for future reference. The digital signal number of bits depends on the oscilloscope buffer size. Large number of bits can be stored using Analog Discovery kit or Xilinx IP core and chipscope software of FPGA [6].

Therefore, taking consideration of above mentioned parameters one could remove distorion and control environmental constraints. Furthure for experimental testing setup of an ASIC is explained in section III.

III. EXPERIMENTAL RESULTS AND COMPARISON

The Functional testing system of Digital and Mixed signal design ASIC is explained in this section. The 48LQFN package ASIC comprises comparator and ADC circuit named as EDU0043. The 16LQFN package ASIC is prototype of Present Lightweight Cryptography algorithm named as EDU0084. Both the ASIC are designed at 180nm CMOS technology operating at 1.8 V power supply. The Keysight MSOX4024A is used to capture the output, Rigol Power supply is used to supply power, and function generator is used to give input signal. The Basys 3 is used to give select signals and plaintext. As proof-of-principle the output results of ADC and comparator are cross-verified on Cadence software tools. The Present Lightweight cryptography is performed on Xilinx Vivado as proof of concept.

Initially, the EDU0043 QFN package is converted in DIP package using QFN to DIP convertor, to make soldering convenient. The experimental setup of comparator comprises of a filter a 100 Ω resistor and 0.1 µF capacitor for impedance matching and a digital buffer 74AUP2G34 as is shown in Figure 3. In comparator the input of reference signal is given through voltage divider, analog and clock signal is given through function generator. The output is seen on MSO as shown in Figure 4 and authenticated from the comparator output in Cadence is shown in Figure 5.

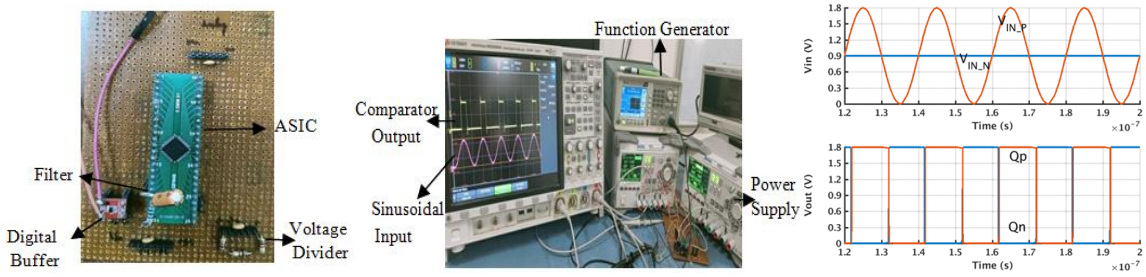
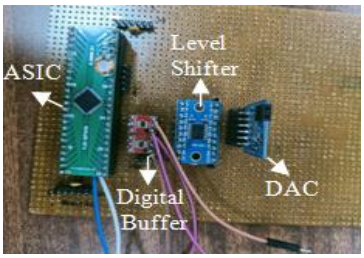


Fig. 3 Comparator ASIC Testing PCB Fig.4 Comparator ASIC Output Fig.5 Comparator Software Output

In Analog-to-Digital Convertor (ADC) testing, impedance matching with 100 Ω resistor and 0.1 µF capacitor is done at analog input which is given from function generator of 5 MHz sinusoidal signal. The analog and digital power supply is given separately. The ADC Testing PCB is shown in Figure 6. At the output digital buffers are used to get the output which is seen at MSO and analog discovery as shown in Figure 7. For the verification, a DAC is given the ADC output after a level shifter as the DAC used works at 3.3V and ADC at 1.8V, so as to check if one gets the same output as input as shown in Figure 8.



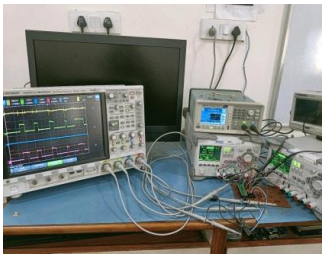
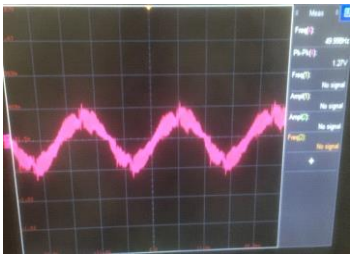
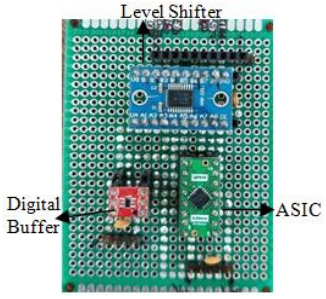



Fig. 6 ADC ASIC Testing PCB Fig.7 ADC ASIC Output Fig.8. ADC Output retrieves from DAC

The Present Crypto ASIC EDU0084 is a 16 pin QFN package which is soldered on DIP package convertor. The Basys 3 FPGA through level shifter gives plaintext (Data + Key), 10MHz Clock and Select signals such as Reset, Key Data Load and Reset. The select signals are controlled through switches on the basys 3.The Led act as a flag for Output is ready. Finally, the Data output is seen at MSO through digital Buffer. The Crypto ASIC Testing PCB is shown in Figure 9. If MSO buffer size is less than one can use Analog Discovery kit to capture the entire 64 bits output as shown in Figure 10. The output data is validated performing simulation on Vivado tool with same plaintext as given while crypto chip testing as shown in Figure 11.



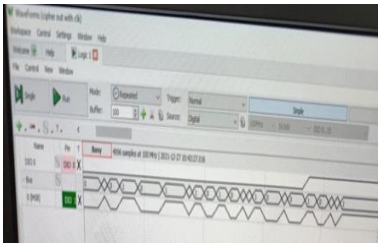
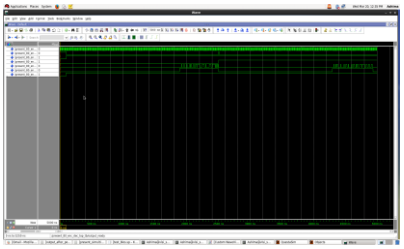



Fig. 9 Crypto ASIC Testing PCB Fig.10 Crypto ASIC Output Fig.11 Crypto Software Output

IV. CONCLUSION AND FUTURE SCOPE

The unique Test Plan for functional testing of an Application Specific Integrated Circuit (ASIC) is explained in the paper. The Test Plan is described using analog, digital and mixed signal design ASIC so as to cover all domains. The testing methodology is divided in two parts before and after PCB designing. The results obtained while ASIC testing are validated by the simulation from software tools. The methodology needs minimal components and with (high) 99% output efficient rate.

The ASICs tested in System Design (Prototype) are beneficial for real time applications. The ADC tested is all digital 6-bit Flash ADC and can be used in Car brakes for clash avoidance. Moreover, the Present crypto ASIC could be used to encrypt the multilingual languages, utilized by layman to protect their data.

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